About this Manual

We've added this manual to the Agilent website in an effort to help you support your product. This manual is the best copy we could find; it may be incomplete or contain dated information. If we find a more recent copy in the future, we will add it to the Agilent website.

Support for Your Product

Agilent no longer sells or supports this product. Our service centers may be able to perform calibration if no repair parts are needed, but no other support from Agilent is available. You will find any other available product information on the Agilent Test & Measurement website, www.tm.agilent.com.

HP References in this Manual

This manual may contain references to HP or Hewlett-Packard. Please note that Hewlett-Packard's former test and measurement, semiconductor products and chemical analysis businesses are now part of Agilent Technologies. We have made no changes to this manual copy. In other documentation, to reduce potential confusion, the only change to product numbers and names has been in the company name prefix: where a product number/name was HP XXXX the current name/number is now Agilent XXXX. For example, model number HP8648A is now model number Agilent 8648A.

User's Guide

Publication Number E2484-97001
March 1998

For Safety Information, Warranties, and Regulatory Information, see the pages at the end of this manual.

HP E2484A Analysis Probe for I960RP

The HP E2484A Analysis Probe — At a Glance

The HP E2484A Analysis Probe provides a complete interface for
state or timing analysis between an i960RP microprocessor and
HP logic analyzers. The supported logic analyzers are listed in
chapter 1.

Supported Microprocessors

| Microprocessor	Package	Voltage
i960RP	352-pin BGA*	3.3 V
i960RP	352-pin BGA*	5 V

* Target system must have P2P connector for attaching the analysis probe.

The analysis probe provides the physical connection between the
target microprocessor and the logic analyzer. The configuration
software on the enclosed disks set up the logic analyzer for
compatibility with the analysis probe. The inverse assemblers on the
disks let you obtain displays of the i960 data bus in i960 assembly
language mnemonics.
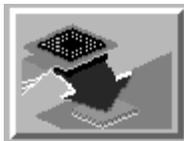
If you are using the analysis probe with the HP 16600 or HP 16700
series logic analysis systems, you only need this manual as a
reference. The HP 16600 and 16700 series contain a Setup Assistant,
which guides you through the connection and configuration process
using on-screen dialog windows. For an overview of of Setup
Assistant, refer to Chapter 1, "Setup Assistant."

For more information on the logic analyzers or microprocessor, refer
to the appropriate reference manuals for those products.

Logic
Analyzer

e2484e07

CAUTION:

Target
System

Analysis
Probe

P2P Adapter
Assembly
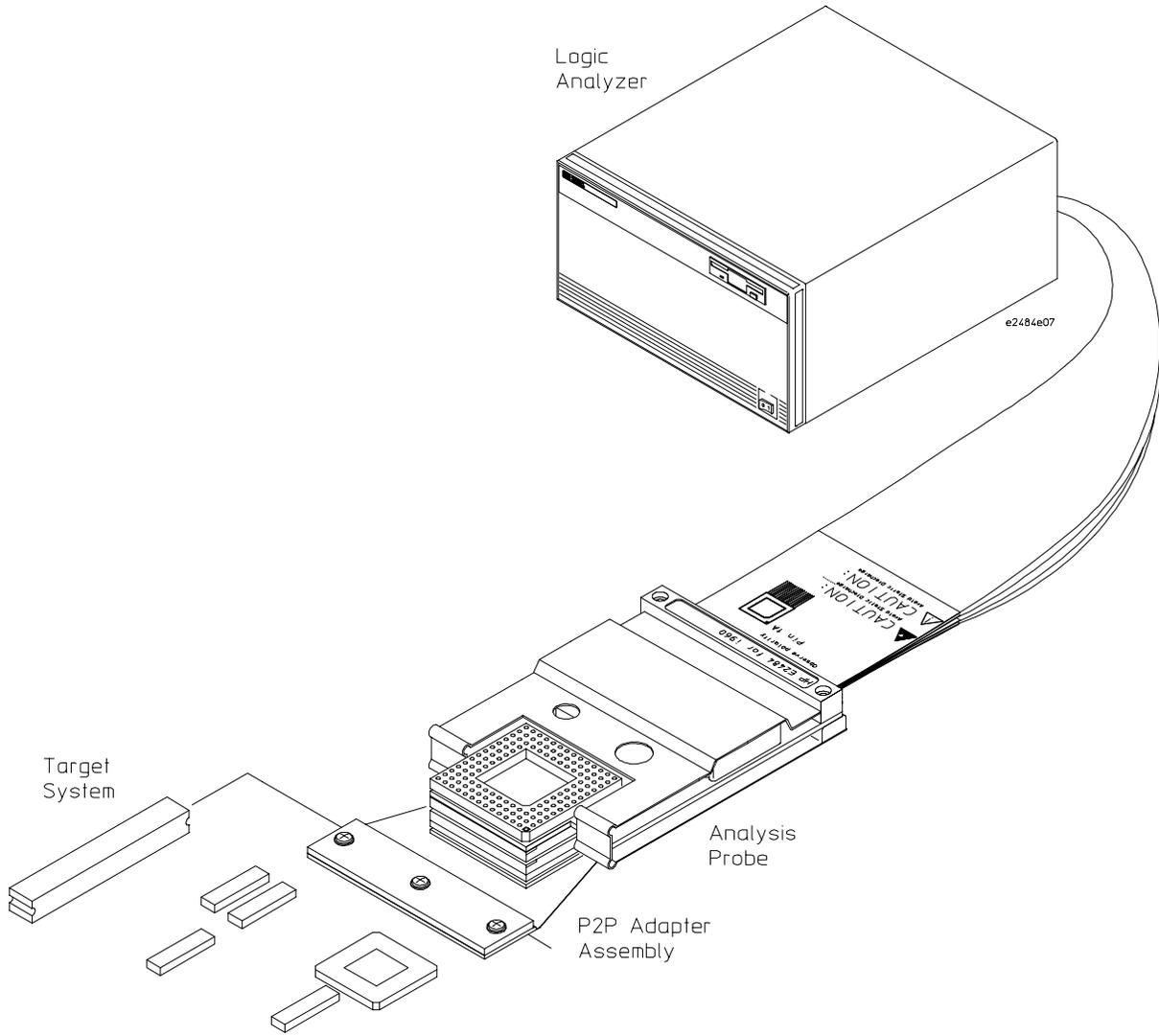
Analyzing a Target System with the HP E2484A Analysis Probe

In This Book

This book is the User's Guide for the HP E2484A Analysis Probe. It assumes that you have a working knowledge of the logic analyzer used and the microprocessor being analyzed.

This user's guide is organized into the following chapters:
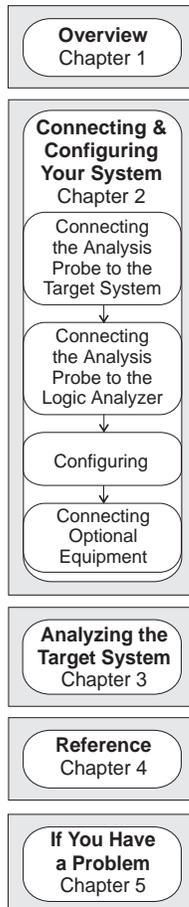
Chapter 1 contains overview information, including a list of required equipment.

Chapter 2 explains how to connect the logic analyzer to your target system through the analysis probe, and how to configure the analysis probe and logic analyzer to interpret target system activity. The last section in this chapter shows you how to hook up optional equipment to obtain additional functionality.

HP 16600 and HP 16700 Series Logic Analysis Systems

If you are using the analysis probe with HP 16600 or HP 16700 series logic analysis systems, you only need this manual as a reference for obtaining and interpreting data. The HP 16600 and HP 16700 contain a Setup Assistant, which guides you through the connection and configuration process using on-screen dialog windows. For an overview of Setup Assistant, refer to chapter 1, "Setup Assistant."

Chapter 3 provides information on analyzing the supported microprocessors.

Chapter 4 contains reference information on the analysis probe.

Chapter 5 contains troubleshooting information.

Contents

1

Overview

Overview

This chapter describes:

- Setup Assistant
- Logic analyzers supported
- Logic analyzer software version requirements
- Equipment used with the analysis probe
- Equipment supplied
- Minimum equipment required
- Additional equipment supported

Overview
Chapter 1

Connecting &
Configuring
Your System
Chapter 2

Connecting
the Analysis
Probe to the
Target System

Connecting
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Probe to the
Logic Analyzer

Configuring

Connecting
Optional
Equipment

Analyzing the
Target System
Chapter 3

Reference
Chapter 4

If You Have
a Problem
Chapter 5
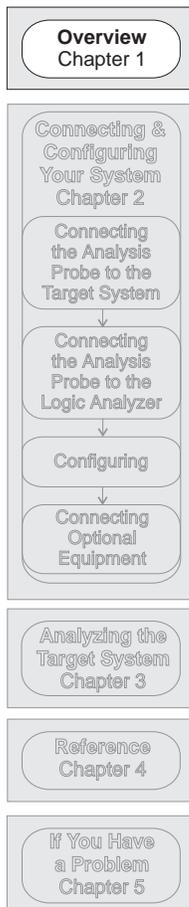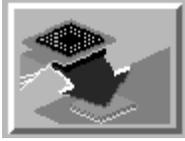
Setup Assistant

Setup Assistant is an online tool for connecting and configuring your logic analysis system for microprocessor and bus analysis. Setup Assistant is available on the HP 16600 and HP 16700 series logic analysis systems. You can use Setup Assistant in place of the connection and configuration procedures provided in chapter 2.

This menu-driven tool will guide you through the connection procedures for connecting the logic analyzer to an analysis probe, an emulation module, or other supported equipment. It will also guide you through connecting an analysis probe to the target system.

Access Setup Assistant by clicking its icon in the Logic Analysis System window. The on-screen dialog prompts you to choose the type of measurements you want to make, the type of target system, and the associated products that you want to set up.

If you ordered this product with your HP 16600/700 logic analysis system, the logic analysis system has the latest software installed, including support for this product. If you received this product after you received your logic analysis system, this product might not be listed under supported products. In that case, you need to install the i960RP Processor Support Package. Use the procedure on the CD-ROM jacket to install the i960RP Processor Support Package.

Logic Analyzers Supported

The table below lists the logic analyzers supported by the HP E2484A analysis probe. Logic analyzer software version requirements are shown on the following page.

The HP E2484A requires five logic analyzer pods (80 channels) for inverse assembly. The analysis probe contains one additional pod that you can monitor.

Logic Analyzers Supported

Logic Analyzer	Channel Count	State Speed	Timing Speed	Memory Depth
16600A	204	100 MHz	125 MHz	64 k states
16601A	136	100 MHz	125 MHz	64 k states
16602A	102	100 MHz	125 MHz	64 k states
16550A (one card)	102/card	100 MHz	250 MHz	4 k states
16554A (two cards)	68/card	70 MHz	125 MHz	512 k states
16555A (two cards)	68/card	110 MHz	250 MHz	1 M states
16555D (two cards)	68/card	110 MHz	250 MHz	2 M states
16556A (two cards)	68/card	100 MHz	200 MHz	1 M states
16556D (two cards)	68/card	100 MHz	200 MHz	2 M states
1660A/AS/C/CS/CP	136	100 MHz	250 MHz	4 k states
1661A/AS/C/CS/CP	102	100 MHz	250 MHz	4 k states
1670A	136	70 MHz	125 MHz	64 k or .5 M states
1670D	136	100 MHz	125 MHz	64 k or 1 M states
1671A	102	70 MHz	125 MHz	64 k or .5 M
1671D	102	100 MHz	125 MHz	64 k or 1 M

Logic analyzer software version requirements

The logic analyzers must have software with a version number greater than or equal to those listed below to make a measurement with the HP E2484A. You can obtain the latest software at the following web site:

www.hp.com/go/logicanalyzer

If your software version is older than those listed, load new system software with the above version numbers or higher before loading the HP E2484A software.

Logic Analyzer Software Version Requirements

Logic Analyzer	Minimum Logic Analyzer Software Version for use with HP E2484A
HP 16600 Series	The latest HP 16600 logic analyzer software version is on the CD ROM shipped with this product.
HP 1660A/AS Series	A.03.01
HP 1660C/CS/CP Series	A.02.01
HP 1670A/D Series	A.02.01
Mainframes*	
HP 16700 Series	The latest HP 16700 logic analyzer software version is on the CD ROM shipped with this product.
HP 16500C Mainframe**	A.01.05
HP 16500B Mainframe**	A.03.14

* The mainframes are used with the HP 16550 and HP 16554/55/56 logic analyzer modules.
** The HP 16505A provides a windowed user interface for the HP 16500B/C Logic Analysis System. Refer to the *HP 16505A Prototype Analyzer Installation Guide* for information on connecting the HP 16505A to the HP 16500B/C Logic Analysis System. The HP 16505A requires software version A.01.30 or higher.

Equipment Used with the Analysis Probe

This section lists equipment used with the analysis probe. This information is organized under the following titles: equipment supplied, minimum equipment required, and additional equipment supported

Equipment supplied

The equipment supplied with the analysis probe is shown in the illustration on the next page. It is listed below:

• The analysis probe, which includes the analysis probe circuit card and cables.

• A P2P adapter assembly, which includes three screws and washers, an electrical interface plate, and a back support.

• Logic analyzer configuration files and inverse assembler software on a 3.5-inch disk.

• Logic analyzer configuration files and inverse assembler software on a CD-ROM.

• HP 16505A prototype analyzer configuration files on a 3.5-inch disk.

• This User's Guide.

Analysis
Probe

Software
and Manual

P2P Adapter Assembly
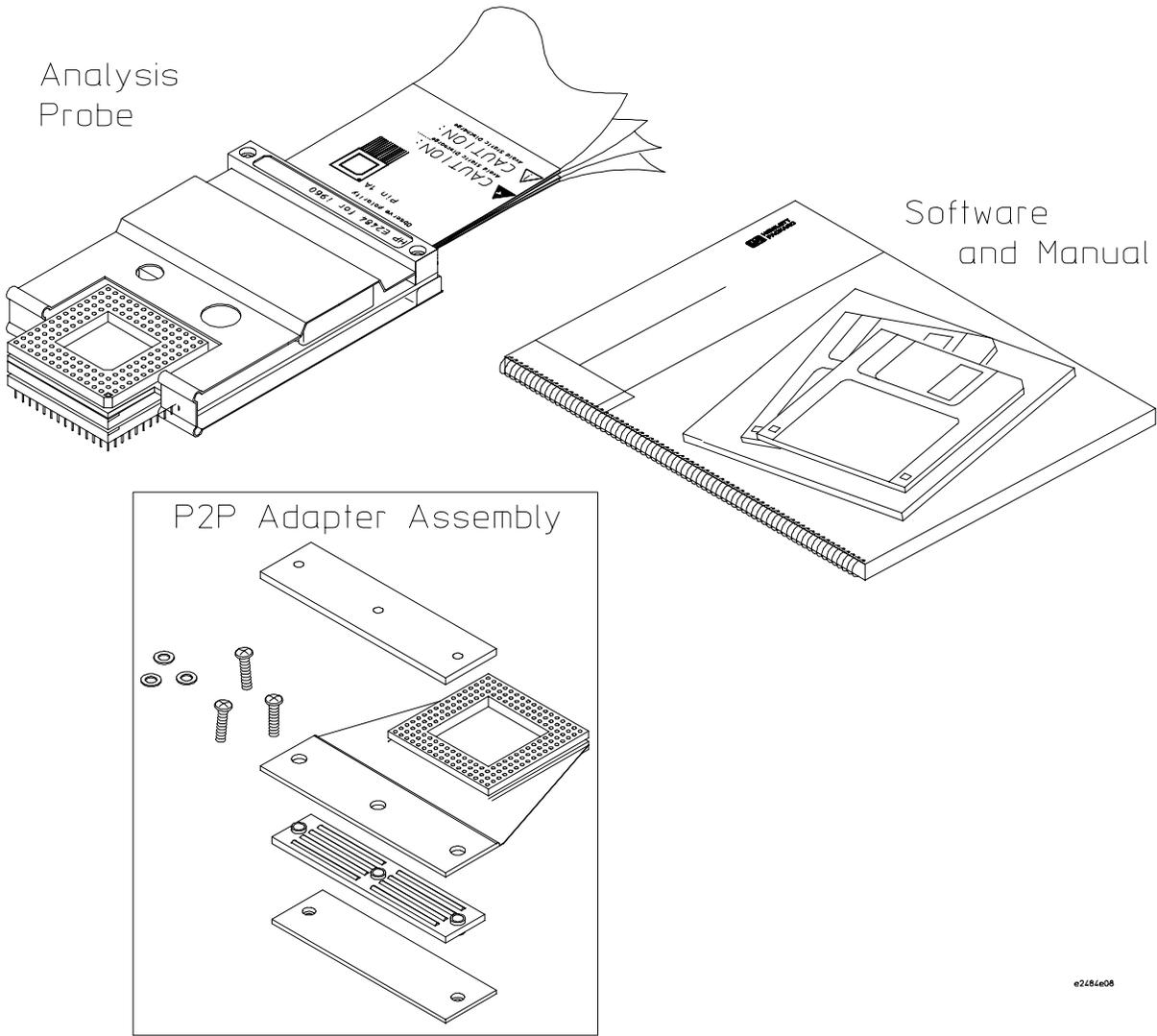
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Equipment Supplied with the HP E2484A

Minimum equipment required

For state and timing analysis of an i960RP target system, you need all of the following items.

- The HP E2484A analysis probe.

- A P2P connector on the target system.

- One of the logic analyzers listed on page 1-4. The logic analyzer software version requirements are listed on page 1-5.

Additional equipment supported

The HP E2484A does not support any additional equipment.

2

Connecting and Configuring Your System

Connecting and Configuring Your System

**Connecting &
Configuring
Your System**
Chapter 2

Connecting
the Analysis
Probe to the
Target System

Connecting
the Analysis
Probe to the
Logic Analyzer

Configuring

Connecting
Optional
Equipment

This chapter shows you how to connect the logic analyzer to the target system through the analysis probe.

If you are connecting to an HP 16600 or HP 16700 series logic analysis system, follow the instructions given on-screen in the Setup Assistant for connecting and configuring your system. Use this manual for additional information, if desired. Refer to chapter 1 for a description of Setup Assistant.

If you are not using the Setup Assistant, follow the instructions given in this chapter. This chapter is divided into the following sections; the order shown here is the recommended order for performing these tasks:

- Read the power on/power off sequence
- Connect the analysis probe to the target system
- Connect the analysis probe to the logic analyzer
- Configure the analysis probe
- Configure the logic analyzer
- Connect optional equipment

Read the power on/power off sequence.

Target System — Analysis Probe

Target System — Analysis Probe — Logic Analyzer

Target System — Analysis Probe — Logic Analyzer

Set Switches

Target System — Analysis Probe — Logic Analyzer — **Configuration Files and Inverse Assembler Files**
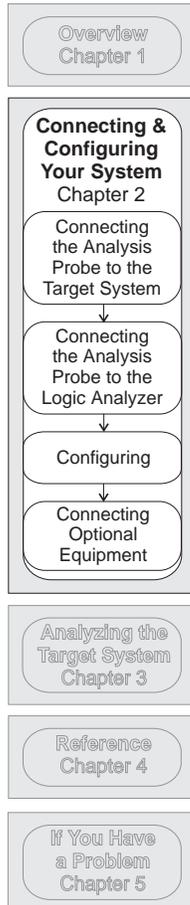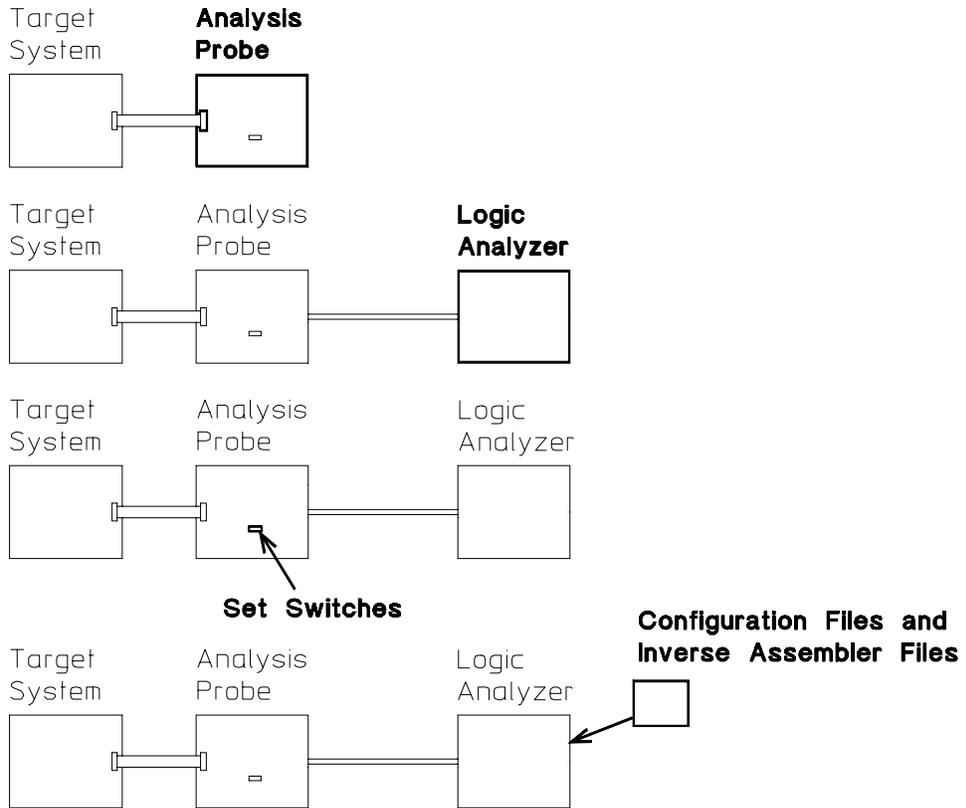
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Connection Sequence

Power-on/Power-off Sequence

Listed below are the sequences for powering on and off a fully connected system. Simply stated, your target system is always the last to be powered on, and the first to be powered off.

To power on HP 16600 and HP 16700 series logic analysis systems

Ensure the target system is powered off.

1 Turn on the logic analyzer. The Setup Assistant will guide you through the process of connecting and configuring the analysis probe.
2 When the analysis probe is connected to the target system and logic analyzer, and everything is configured, turn on your target system.

To power on all other logic analyzers

With all components connected, power on your system in the following order:

1 Logic analysis system.
2 Your target system.

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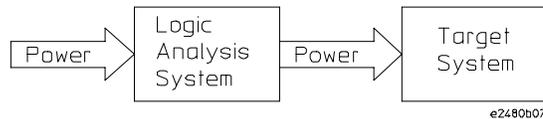
To power off

Turn off power to your system in the following order:

1 Turn off your target system.
2 Turn off your logic analysis system.

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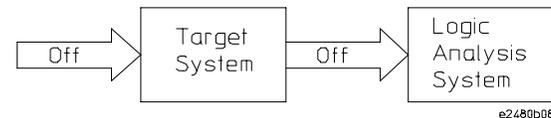
Connecting the Analysis Probe to the Target System
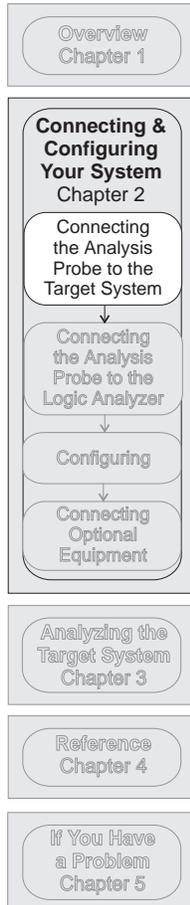
This section explains how to connect the HP E2484A analysis probe to the target system. Connecting the analysis probe to the target system consists of the following tasks:

- Install the P2P connector on the target system.
- Connect the analysis probe to the P2P connector.

The remainder of this section describes these general tasks in more detail.

Protect Your Equipment

The analysis probe socket assembly pins are covered for shipment with a conductive foam wafer or conductive plastic pin protector. This is done to protect the delicate gold-plated pins from damage due to impact. When you are not using the analysis probe, protect the socket assembly pins from damage by covering them with the pin protector.

To connect the P2P adapter to the target system

CAUTION	**Equipment Damage.** To prevent equipment damage, remove power from the target system and make sure no logic analyzer cables are connected to the analysis probe.

The P2P adapter assembly connects to a P2P connector on the target system (see figure on next page), and the analysis probe connects to the P2P adapter assembly. Plastic pin protector sockets can be added between the analysis probe and the P2P adapter assembly for increased clearance.

1 To prevent equipment damage, remove power from both the logic analyzer and the target system.

2 Using a flat-head screwdriver, remove the three screws from the P2P adapter assembly. Position the bottom plastic support underneath the target system, place the P2P adapter on top of the P2P connector with the electrical pads making contact, and place the top plastic support on top of the P2P adapter. Tighten the screws with 2 ft-lbs of torque.

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Connecting the P2P Adapter to the Target System

To connect the analysis probe to the P2P adapter

CAUTION

Equipment Damage. To prevent equipment damage, remove power from the target system and make sure no logic analyzer cables are connected to the analysis probe.

Connect the analysis probe to the P2P adapter as shown on the following page. Note the orientation of the analysis probe with respect to the P2P adapter.

CAUTION

Incorrect Connection. Serious damage to the target system or analysis probe can result from incorrect connection. Note the orientation of the analysis probe with respect to the P2P adapter shown in the figure on the next page. Also, take care to align the analysis probe connector with the pins on the P2P adapter socket so that all pins are making contact.

If the analysis probe connector interferes with components of the target system or if a higher profile is required, additional plastic pin protector sockets can be added. Plastic pin protector sockets can be ordered from Hewlett-Packard using the part number 1200-1605. However, any 132-pin PGA IC socket and gold-plated pins can be used.

Pin A1

e2484e04

HP E2484A Analysis Probe and P2P Adapter

Connecting the Analysis Probe to the Logic Analyzer
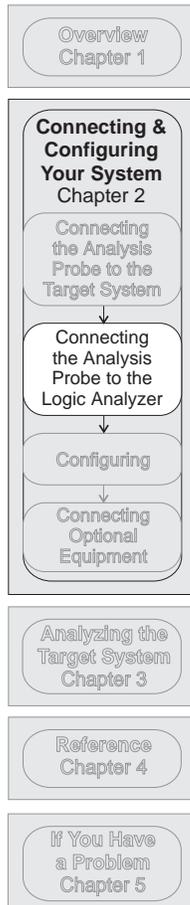
The following sections show the connections between the logic analyzer pod cables and the analysis probe cables. Use the appropriate section for your logic analyzer. The configuration file names for each logic analyzer are located at the bottom of the connection diagrams.

A minimum of five analysis probe pods are required for inverse assembly (P1, P2, P3, P4, and P5). P6 contains additional status signals which may be useful for microprocessor analysis. The figure on the following page shows the pod locations on the analysis probe.

This section shows connection diagrams for connecting the analysis probe to the logic analyzers listed below:

- HP 16600A logic analysis system
- HP 16601A logic analysis system
- HP 16602A logic analysis system
- HP 16550A logic analyzer (one card)
- HP 16554/55/56 logic analyzers (two cards)
- HP 1660A/AS/C/CS/CP logic analyzers
- HP 1661A/AS/C/CS/CP logic analyzers
- HP 1670A/D logic analyzers
- HP 1671A/D logic analyzers

Analysis probe pod locations

The illustration below shows the pod locations on the analysis probe.
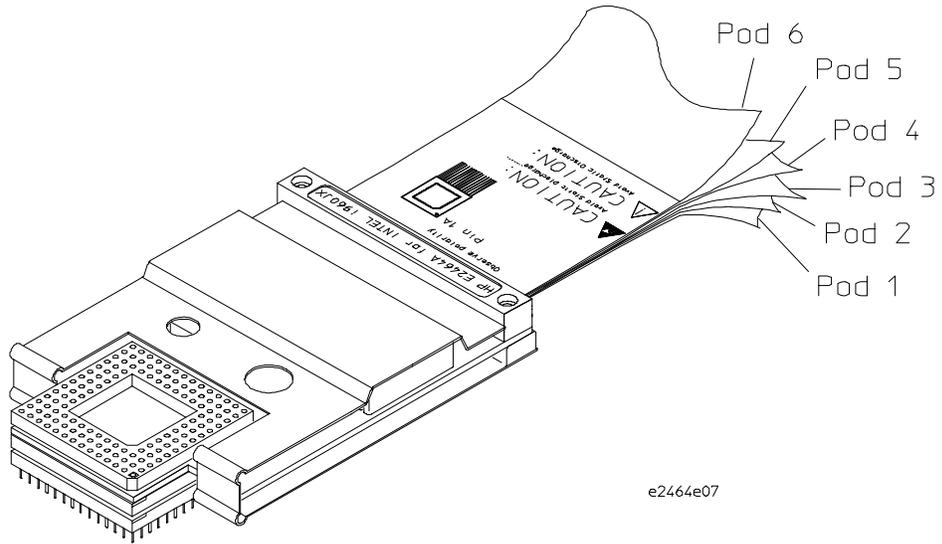
HP E2484A Analysis Probe Pod Locations

To connect to the HP 16600A logic analysis system

Use the figure and table below to connect the analysis probe to the
HP 16600A logic analysis system.

POD 11
POD 12
POD 9
POD 10

Not Used

POD 1
POD 2
POD 3
POD 4
POD 5
POD 6
POD 7
POD 8
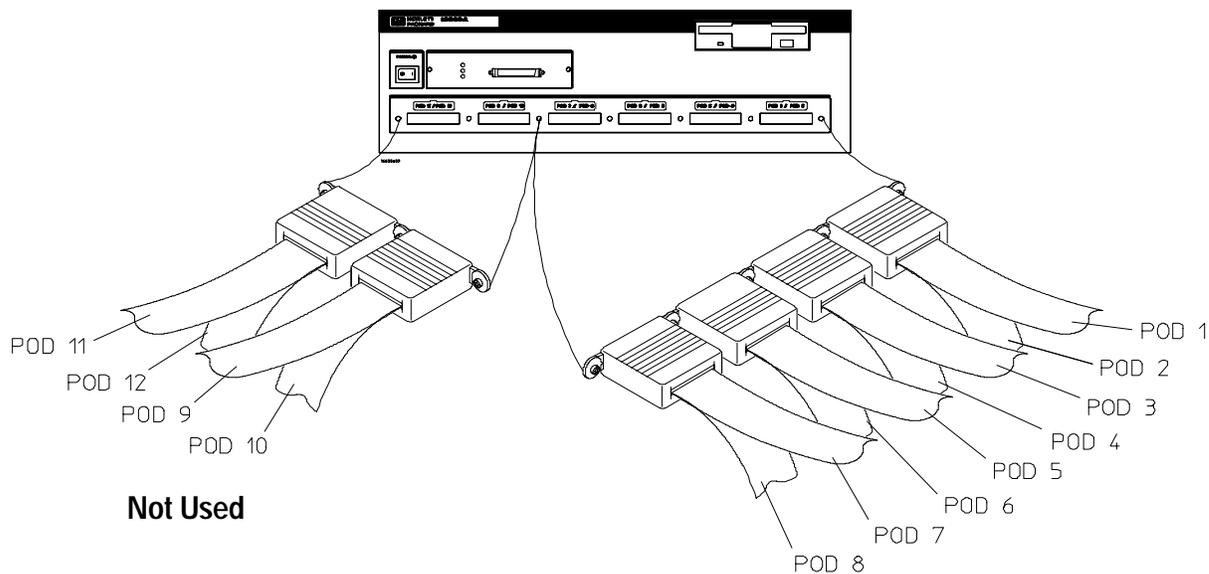
HP 16600	Pod 8	Pod 7	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
HP E2484A Connector	P6 other	P5 STAT	not used	not used	P4 DATA	P3 DATA	P2 ADDR	P1 ADDR clk ⇕

Configuration File
Use configuration file C960R_02 for the HP 16600 logic analyzer.

To connect to the HP 16601A logic analysis system

Use the figure and table below to connect the analysis probe to the
HP 16601A logic analysis system.
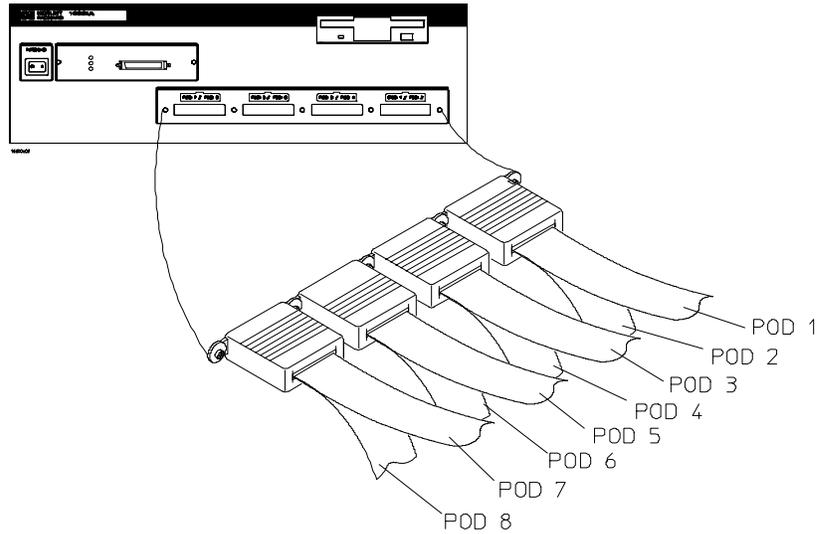
HP 16601	Pod 8	Pod 7	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
HP E2484A Connector	P6 other	P5 STAT	not used	not used	P4 DATA	P3 DATA	P2 ADDR	P1 ADDR clk ⇕

> **Configuration File**
> Use configuration file C960R_02 for the HP 16601 logic analyzer.

To connect to the HP 16602A logic analysis system

Use the figure and table below to connect the analysis probe to the
HP 16602A logic analysis system.

HP 16602	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
HP E2484A Connector	P6 other	P5 STAT	P4 DATA	P3 DATA	P2 ADDR	P1 ADDR clk ⇕

Configuration File
Use configuration file C960R_01 for the HP 16602 logic analyzer.

To connect to the HP 16550A logic analyzer

Use the figure and table below to connect the analysis probe to the
HP 16550A logic analyzer.

HP 16550A
Expansion Card

HP 16550A
Master Card
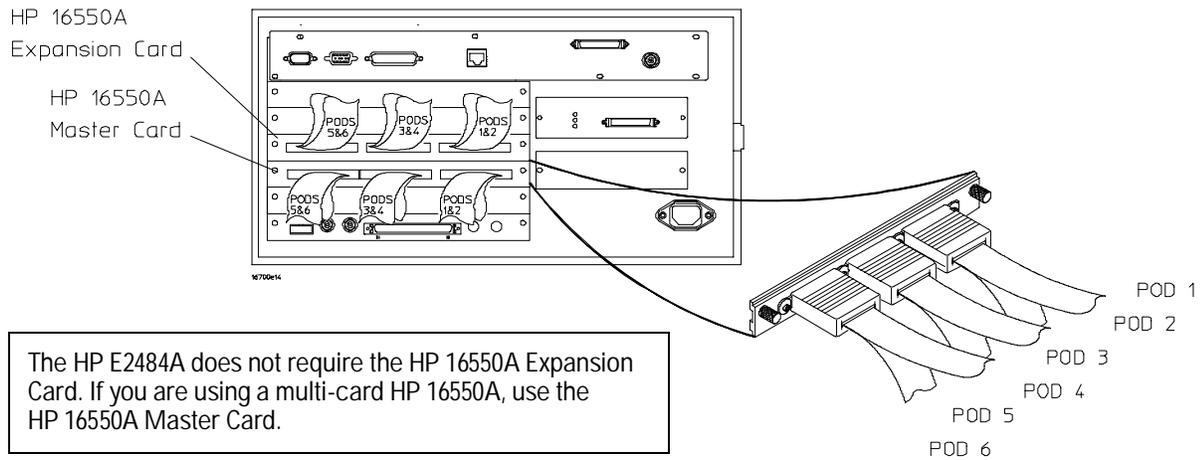
The HP E2484A does not require the HP 16550A Expansion
Card. If you are using a multi-card HP 16550A, use the
HP 16550A Master Card.

HP 16550A Master Card	Master Card Pod 6	Master Card Pod 5	Master Card Pod 4	Master Card Pod 3	Master Card Pod 2	Master Card Pod 1
HP E2484A Connector	P6 other	P5 STAT	P4 DATA	P3 DATA	P2 ADDR	P1 ADDR clk ↕

Configuration File
Use configuration file C960R_01 for the HP 16550A logic analyzer.

To connect to the HP 16554/55/56 logic analyzers

Use the figure and table below to connect the analysis probe to the
HP 16554A/55A/56A and HP 16555D/56D logic analyzers.
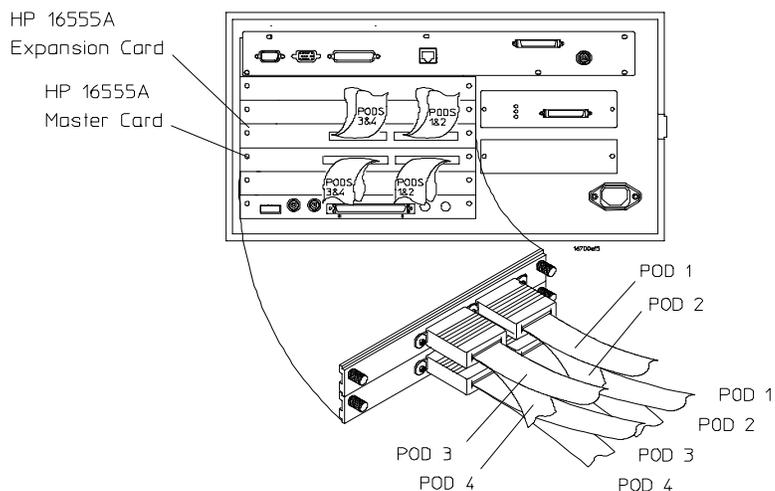
HP 16554/55/56 Exp. Card 1	Expansion Card 1 Pod 4	Expansion Card 1 Pod 3	Expansion Card 1 Pod 2	Expansion Card 1 Pod 1
HP E2484A Connector	not used	not used	P6 other	P5 STAT
HP 16554/55/56 Master Card	Master Card Pod 4	Master Card Pod 3	Master Card Pod 2	Master Card Pod 1
HP E2484A Connector	P4 DATA	P3 DATA	P2 ADDR	P1 ADDR clk ⇕

> **Configuration File**
> Use configuration file C960R_03 for the HP 16554/55/56 logic analyzers.

To connect to the HP 1660A/AS/C/CS/CP logic analyzers

Use the figure and table below to connect the analysis probe to the HP 1660A/C logic analyzers.
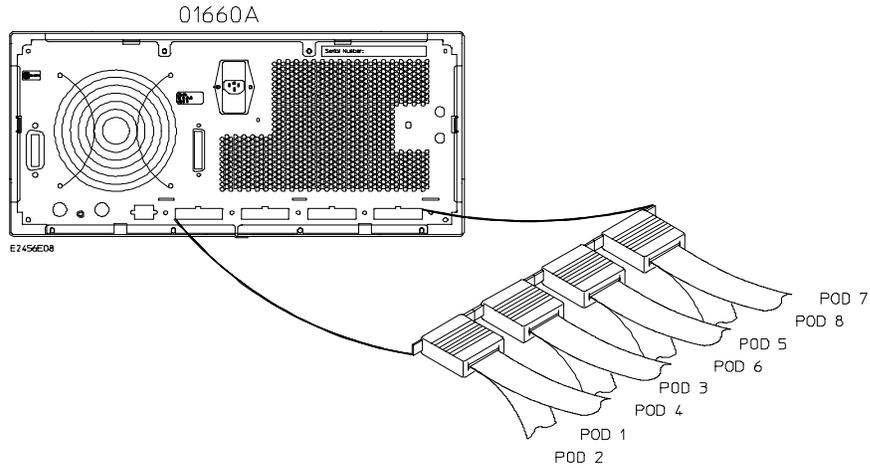
HP 1660A/C	Pod 1	Pod 2	Pod 3	Pod 4	Pod 5	Pod 6	Pod 7	Pod 8
HP E2484A Connector	P1 ADDR clk ⇕	P2 ADDR	P3 DATA	P4 DATA	not used	not used	P5 STAT	P6 other

---

Configuration File
Use configuration file C960R_02 for the HP 1660A/AS/C/CS/CP logic analyzers.

To connect to the HP 1661A/AS/C/CS/CP logic analyzers

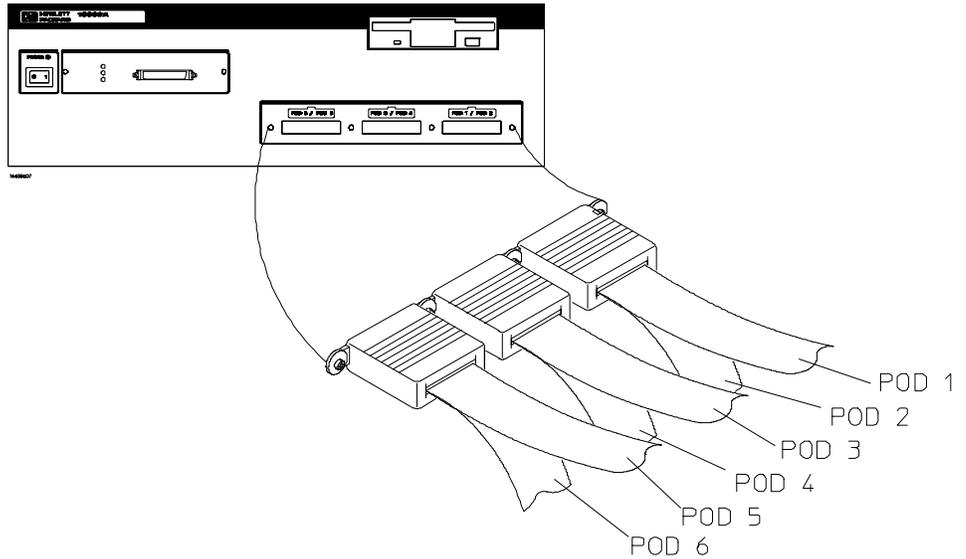Use the figure and table below to connect the analysis probe to the HP 1661A/C logic analyzers.
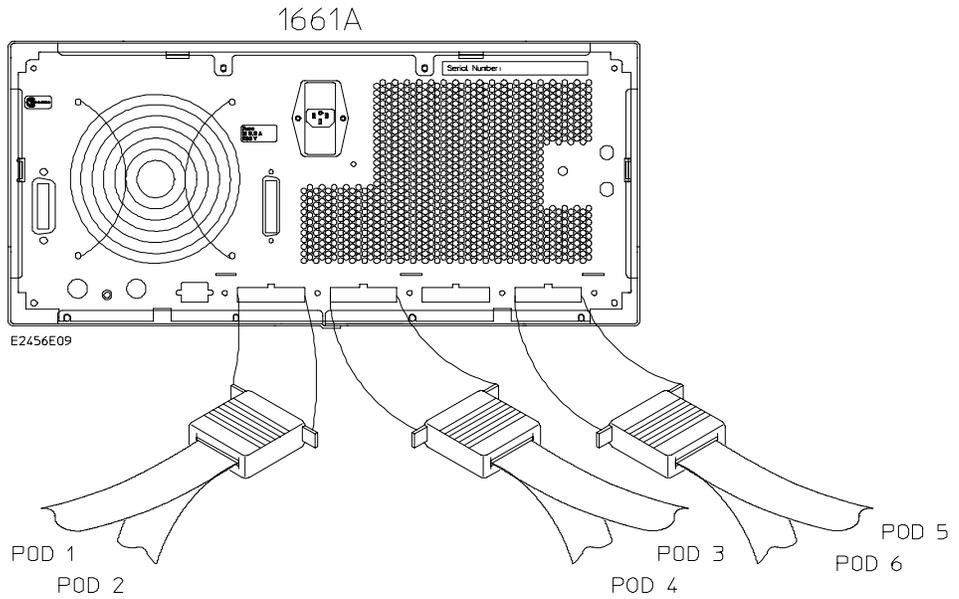
HP 1661A/C	Pod 1	Pod 2	Pod 3	Pod 4	Pod 5	Pod 6
HP E2484A Connector	P1 ADDR clk ↕	P2 ADDR	P3 DATA	P4 DATA	P5 STAT	P6 other

> **Configuration File**
> Use configuration file C960R_01 for the HP 1661A/AS/C/CS/CP logic analyzers.

To connect to the HP 1670A/D logic analyzer

Use the figure and table below to connect the analysis probe to the
HP 1670A/D logic analyzers.

e2465e01
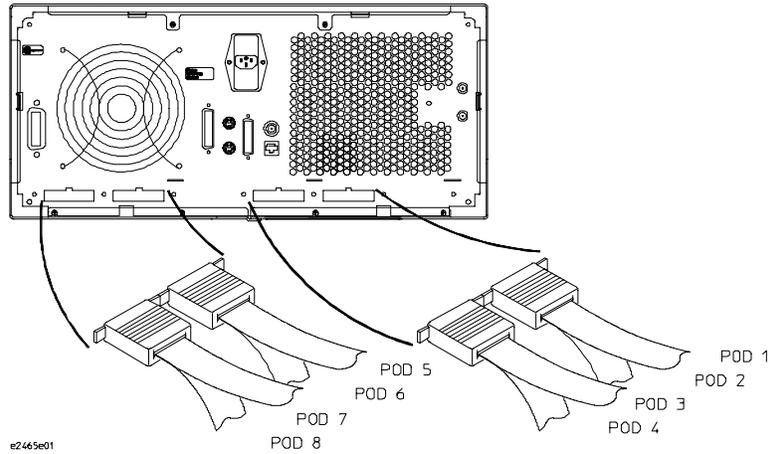
HP 1670A/D	Pod 8	Pod 7	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
HP E2484A Connector	P6 other	P5 STAT	not used	not used	P4 DATA	P3 DATA	P2 ADDR	P1 ADDR clk ⇕

> **Configuration File**
> Use configuration file C960R_02 for the HP 1670A/D logic analyzer.

To connect to the HP 1671A/D logic analyzer

Use the figure and table below to connect the analysis probe to the HP 1671A/D logic analyzer.
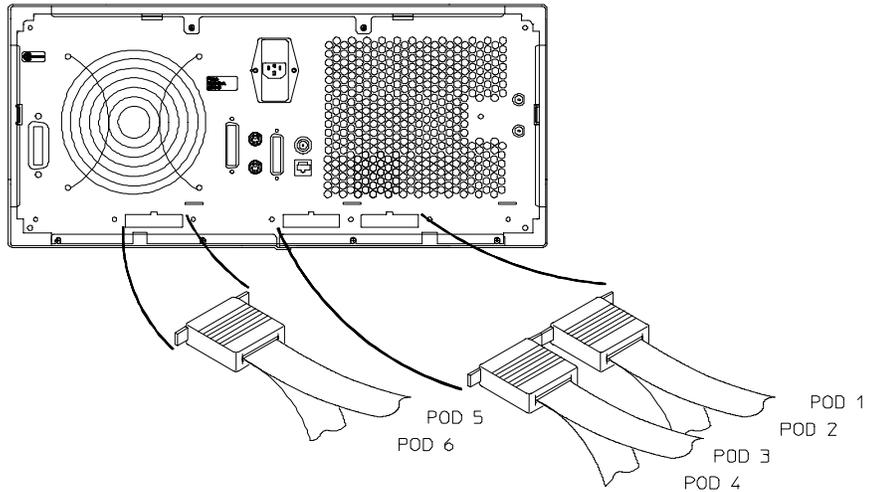
e2473e05

HP 1671A/D	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
HP E2484A Connector	P6 other	P5 STAT	P4 DATA	P3 DATA	P2 ADDR	P1 ADDR clk $\Updownarrow$

Configuration File
Use configuration file C960R_01 for the HP 1671A/D logic analyzer.

Configuring

This section shows you how to configure the HP E2484A Analysis Probe and the logic analyzer. It consists of the following tasks:

- Configuring the analysis probe
- Configuring the logic analyzer
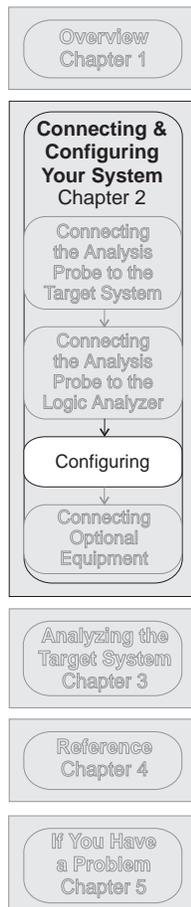
Configuring the Analysis Probe

Configuring the analysis probe consists of the following:

- Setting the State/Timing switch
- Setting the Frequency Range switch

The State/Timing switch and the Frequency Range switch are shown in the illustration on the following page.

To set the State/Timing switch

The analysis probe can operate in three modes: State-per-transfer, State-per-clock, or Timing. The State/Timing switch selects the mode.

1 For State-per-transfer or State-per-clock analysis, set the State/Timing switch to State.

In State mode, the active devices on the analysis probe latch and align the Address, Data, and Status when the processor bus contains valid data. Inverse assembly is not available in State-per-clock mode. Note that you must go to the Format menu and change the clocking to switch between State-per-transfer and State-per-clock modes. See Chapter 3, "Modes of Operation" for additional information.

2 For Timing analysis, set the State/Timing switch to Timing.

In Timing mode, the active devices act as flow-through buffers. Inverse assembly is not available in Timing mode.

See Chapter 3, "Modes of Operation" for additional information on the operating modes.

To set the Frequency Range switch

Switch 1 selects the frequency range. Set it to HIGH if the CPU clkin frequency is 10 MHz or higher and set it to LOW if the frequency is below 10 MHz.
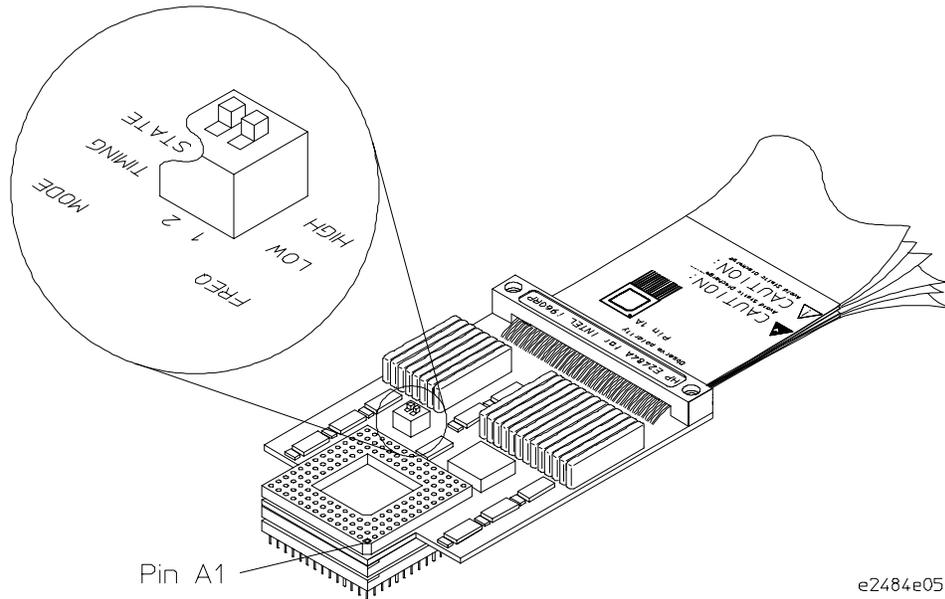
e2484e05

State/Timing and Frequency Range Switches

Configuring the Logic Analysis System

You configure the logic analyzer by loading a configuration file. The information in the configuration file includes:

- Label names and channel assignments for the logic analyzer
- Inverse assembler file name

The configuration file you use is determined by the logic analyzer you are using. The configuration file names are listed with the logic analyzer connection tables, and in a table at the end of this section.

The procedures for loading a configuration file depend on the type of logic analyzer you are using. There is one procedure for the HP 16600/700 series logic analysis systems, and another procedure for the HP 1660-series, HP 1670-series, and logic analyzer modules in an HP 16500B/C mainframe. Use the appropriate procedures for your analyzer.

To load configuration and inverse assembler files — HP 16600/700 logic analysis systems

If you did not use Setup Assistant, you can load the configuration and inverse assembler files from the logic analysis system hard disk.

1 Click on the File Manager icon. Use File Manager to ensure that the subdirectory /hplogic/configs/hp/i80960rp/ exists.

> If the above directory does not exist, you need to install the i960RP Processor Support Package. Close File Manager, then use the procedure on the CD-ROM jacket to install the i960RP Processor Support Package before you continue.

2 Using File Manager, select the configuration file you want to load in the /hplogic/configs/hp/i80960rp/ directory, then click Load. If you have more than one logic analyzer installed in your logic analysis system, use the Target field to select the machine you want to load.

The logic analyzer is configured for i960RP analysis by loading the appropriate configuration file. Loading this file also automatically loads the enhanced inverse assembler.

3 Close File Manager.

To load configuration and inverse assembler files — other logic analyzers

If you have an HP 1660-series, HP 1670-series, or logic analyzer modules in an HP 16500B/C mainframe use these procedures to load the configuration file and inverse assembler.

The first time you set up the analysis probe, make a duplicate copy of the master disk. For information on duplicating disks, refer to the reference manual for your logic analyzer.

For logic analyzers that have a hard disk, you might want to create a directory such as 960RP on the hard drive and copy the contents of the floppy onto the hard drive. You can then use the hard drive for loading files.

1 Insert the floppy disk in the front disk drive of the logic analyzer.

2 Go to the Flexible Disk menu.

3 Configure the menu to load.

4 Use the knob to select the appropriate configuration file.

Choosing the correct configuration file depends on which analyzer you are using. The configuration files are shown with the logic analyzer connection tables, and are also in the table on the next page.

5 Select the appropriate analyzer on the menu. The HP 16500 logic analyzer modules are shown in the Logic Analyzer Configuration Files table.

6 Execute the load operation on the menu to load the file into the logic analyzer.

The logic analyzer is configured for i960RP analysis by loading the appropriate configuration file. Loading this file also automatically loads the enhanced inverse assembler.

Logic Analyzer Configuration Files

Analyzer Model	Analyzer Description (modules only)	Configuration File
16600A	--	C960R_02
16601A	--	C960R_02
16602A	--	C960R_01
16550A (one card)	100 MHz STATE 500 MHz TIMING	C960R_01
16554A (two card)	0.5M SAMPLE 70/125 MHz LA	C960R_03
16555A (two card)	1.0M SAMPLE 110/250 MHz LA	C960R_03
16555D (two card)	2.0M SAMPLE 110/250 MHz LA	C960R_03
16556A (two card)	1.0M SAMPLE 100/200 MHz LA	C960R_03
16556D (two card)	2.0M SAMPLE 100/200 MHz LA	C960R_03
1660A/AS/C/CS	--	C960R_02
1661A/AS/C/CS	--	C960R_01
1670A/D	--	C960R_02
1671A/D	--	C960R_01

Connecting Optional Equipment

The HP E2484A does not support any additional equipment.

3
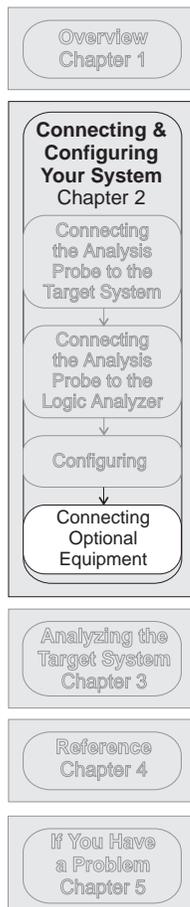
Analyzing the Target System

Analyzing the Target System

This chapter describes modes of operation for the HP E2484A
Analysis Probe. It also describes analysis probe data, symbol
encodings, and information about the inverse assemblers.

The information in this chapter is presented in the following sections:

- Modes of operation
- Logic analyzer configuration
- Using the inverse assemblers

Overview
Chapter 1

Connecting &
Configuring
Your System
Chapter 2

Connecting
the Analysis
Probe to the
Target System

Connecting
the Analysis
Probe to the
Logic Analyzer

Configuring

Connecting
Optional
Equipment

**Analyzing the
Target System**
Chapter 3

Reference
Chapter 4

If You Have
a Problem
Chapter 5
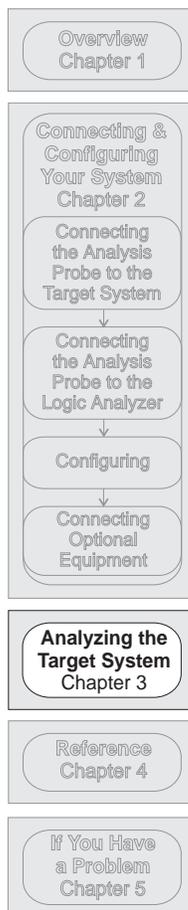
Modes of Operation

The HP E2484A analysis probe can be used in three different analysis modes: State-per-transfer, State-per-clock, and Timing. The following sections describe these operating modes.

State-per-transfer mode

In state-per-transfer mode, data and status are constantly captured on the rising edge of the CPU clock. Address is captured from the data latches and retained on the second level latch upon the assertion of address strobe signal. When valid data appear, which is indicated by the combination of data enabled and ready received asserted low, a Jclk is generated to the logic analyzer. Jclk on the logic analyzer is set to capture on both rising and falling edges of the clock. The analysis probe operates in this manner regardless of whether the bus cycle is a DMA cycle or not. During DMA cycles, it is required that the target drives ADS# instead of ALE or ALE#.

State-per-clock mode

The HP E2484A analysis probe normally clocks the logic analyzer on every rising edge of the microprocessor clock, but only during valid data transfers. State-per-clock mode clocks the logic analyzer on every microprocessor rising clock edge regardless of whether or not a valid data transfer occurs; therefore, every state that crosses the target system microprocessor's bus is captured. This allows the logic analyzer to capture address states, wait states, idle states, and recovery states, in addition to the data states. Inverse assembly is not supported in state-per-clock mode.

In State-per-clock mode Kclk is used instead of Jclk, and it is set to capture only on the rising edge of the clock. Kclk is a no-delay duplicate clock of the CPU clkin. In this mode, the address bus information is the same as that of data bus except lagging by one state. This is the result of having two-levels deep latches to demultiplex the AD[31:0] bus. To select the state-per-clock mode, change the Clock Description in the Format menu from "J clock rising and falling" to "K clock rising." The default mode (clocking only for valid data transfers) uses the J clock rising and falling.

The figure below shows a typical State-per-clock listing. In this example
there are eight wait states between ADS and the first READY.

State-per-clock Listing

Timing mode

In timing mode, all signals are flow-through and have approximately 1-ns channel-to-channel skew. The address signals lag the data signals by about 4 ns since the address signals have to go through two buffers instead of one. Chapter 4 has a Timing waveform diagram.

In Timing mode, all signals have a 4-ns delay with respect to the CPU signals except for TMS, TDO, TDI, and TCLK which have 0-ns delay.

The same format specification loaded for state analysis is also used for timing analysis. To configure the logic analyzer for timing analysis:

1 Configure the HP E2484A for timing analysis by setting the State/Timing switch to TIMING.

2 Select the Configuration menu of the logic analyzer.

3 Select the Type field for the analyzer and select Timing.

Logic Analyzer Configuration

The following sections describe the logic analyzer configuration as set up by the configuration files.

Trigger specification

The trigger specification is set up by the software to store all states. If you modify the trigger specification to store only selected bus cycles, prefetch markings may be incorrect.

Unwanted triggers

The logic analyzer captures prefetches, even if they are not executed. Care must be taken when you are specifying a trigger condition or a storage qualification that follows an instruction that may cause branching. An unused prefetch may generate an unwanted trigger.

Since the microprocessor only prefetches at most four words, one technique to avoid unwanted triggering from unused prefetches is to add "10 hex" to the trigger address. This trigger condition will only be satisfied if the branch is not taken.

DMA cycles

The i960RP microprocessors have two functionally-equivalent output signals to indicate the beginning of a bus cycle, ADS# and ALE. The analysis probe uses ADS# for its internal state machine. Regardless of which of the two signals the target system uses, the analysis probe will always be able to detect the beginning of the bus cycle from ADS#.

During DMA cycles, it is required that ADS# be used by the target system and not ALE. If ALE is used instead of ADS#, only the data and status are captured. To filter out DMA cycles in the state-per-clock or state-per-transfer mode, configure the trigger menu to store only "≠ HLDA".
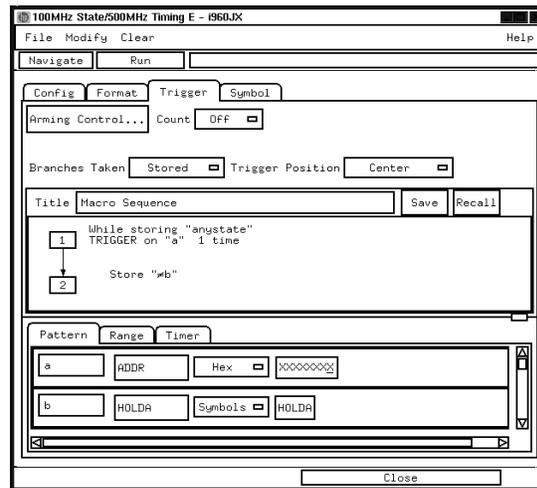
Triggering Sequence for Filtering DMA Cycles

Format specification

The format specification set up by the software is configured for 3.5 ns setup/0 ns hold.

The configuration files contain predefined format specifications. These format specifications include all labels for monitoring the microprocessor and any coprocessors connected directly to the microprocessor. The tables on the following pages show the signals used in the STAT label and the predefined symbols set up by the configuration files.

Do not modify the ADDR, DATA, or STAT labels in the format specification if you want inverse assembly. Changes to these labels may cause incorrect or incomplete inverse assembly.

The following figure shows the Format specification display. There may be some differences in the display shown by your particular analyzer.
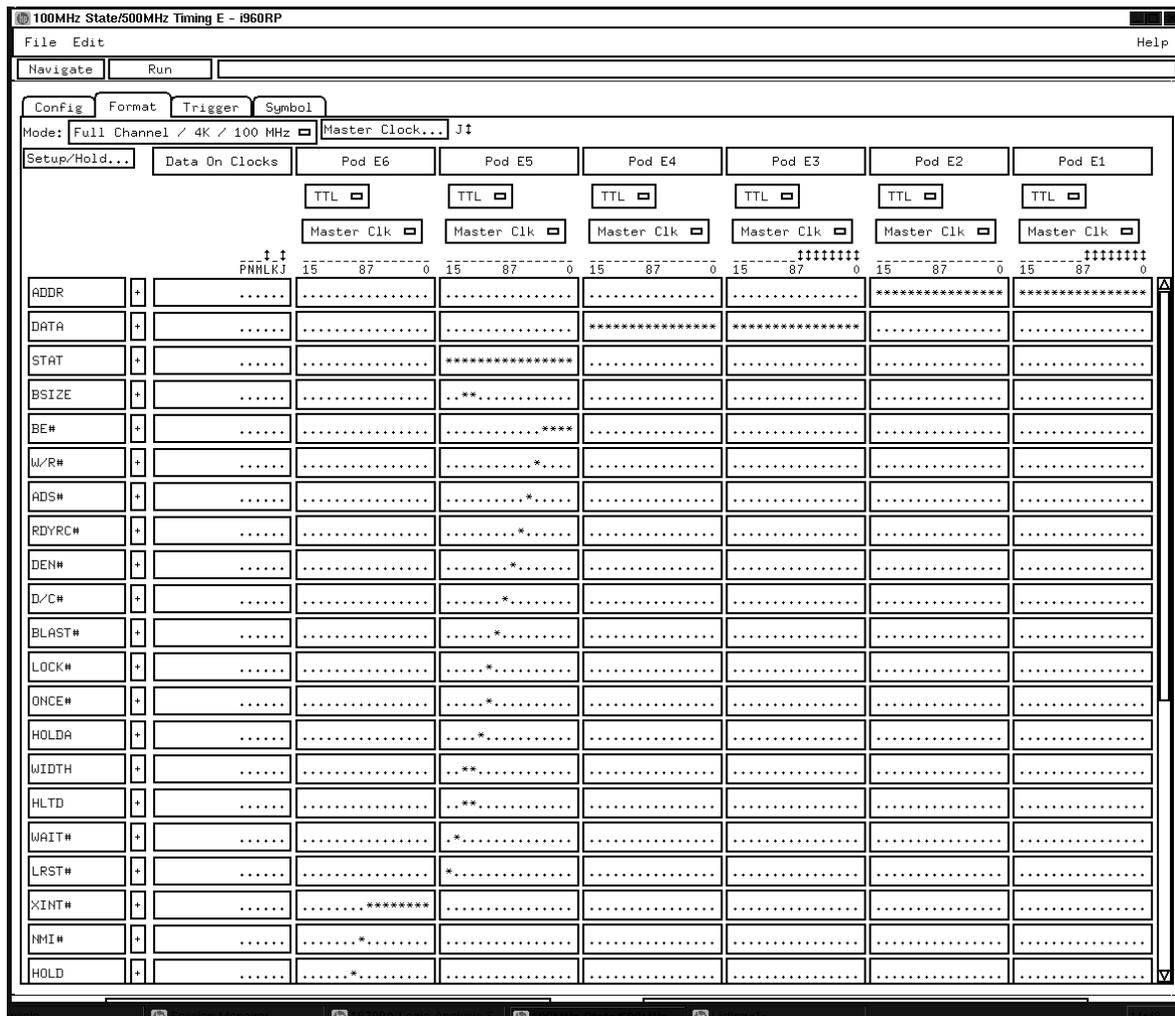
Format Specification

Status Encoding

Each of the bits of the STAT label is described in the table below.

i960RP STAT Label Signal Descriptions

Signal	I/O	Description
AD31:0	I/O	Address/Data Bus.
ALE	O	Address Latch Enable indicates the transfer of a physical address.
ADS#	O	Address Strobe indicates a valid address and the start of a new bus access.
BE3:0#	O	Byte Enables select the byte on the data bus that is valid.
WIDTH/HLTD1:0	I/O	These two signals denote the physical memory attributes for a bus transaction.
D/C#	O	Data/Code indicates that a bus access is a data access or an instruction access.
W/R#	O	Write/Read specifies whether the operation is a write or read.
DT/R#	O	Data Transmit/Receive indicates the direction of data transfer to and from the address/data bus.
DEN#	O	Data Enable indicates data transfer during a bus access.
BLAST#	O	Burst Last indicates the last transfer in a bus access. BLAST# is asserted in the last data transfer of burst and non-burst accesses.
RDYRCV#	I	Ready/Recover indicates that data on AD lines can be sampled or removed.
LOCK#/ONCE#	I/O	Bus Lock indicates that an atomic read-modify-write operation is in progress.
HOLD	I	HOLD is a request from an external bus master to acquire the bus.
HOLDA	O	Hold Acknowledge indicates to an external bus master that the processor has relinquished control of the bus.
CLKIN	I	Clock Input provides the processor's fundamental time base.
RESET#	I	Reset initializes the processor and clears its internal logic.
STEST	I	Self Test enables or disables the processor's internal self-test feature at initialization.
FAIL#	O	Fail indicates a failure of the processor's built-in self-test performed during initialization.
TCK	I	Test Clock is a CPU input which provides the clocking function for Boundary Scan Testing (JTAG).
TDI	I	Test Data Input is the serial input pin for JTAG.
TDO	O	Test Data Output is the serial output pin for JTAG.

i960RP STAT Label Signal Descriptions

Signal	I/O	Description
TRST#	I	Test Reset asynchronously resets the Test Access Port controller function of Boundary Scan testing (JTAG).
TMS	I	Test Mode Select is sampled at the rising edge of TCK to select the operation of the test logic of Boundary Scan testing.
XINT7:0#	I	External Interrupt pins are used to request interrupt service.
NMI#	I	Non-Maskable Interrupt causes a non-maskable interrupt event to occur.
WAIT#	O	WAIT# allows a DMA controller to insert wait states during DMA acesses to an external memory system.

Logic Analyzer Symbols

The HP E2484A configuration software sets up symbol tables on the logic analyzer. The tables contain alphanumeric symbols which identify data patterns or ranges. Labels have been defined in the format specification menu to make triggering on specific cycles easier. The label base in the symbols menu is set to hexadecimal to conserve space in the listing menu. The following figure shows the symbols for the BSIZE label. The table on the following page shows the rest of the labels and symbols.
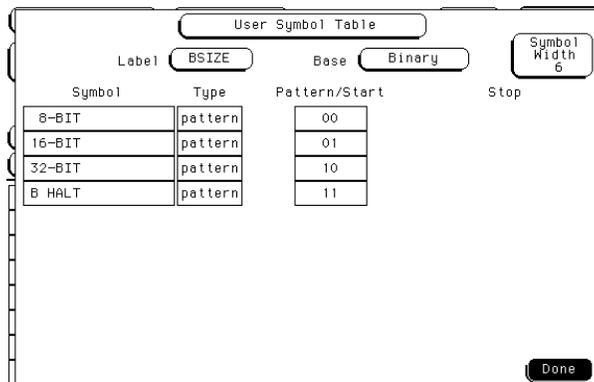
Symbols

i960RP Labels and Symbols

Label	Symbol	Status Encoding	Label	Symbol	Status Encoding
BSIZE	8-BIT	00	ONCE#	ONCE	0
	16-BIT	01		(blank)	1
	32-BIT	10	HOLDA	(blank)	0
	B HALT	11		HOLDA	1
W/R#	READ	0	ALE	(blank)	0
	WRITE	1		ALE	1
ADS#	ADS	0	RESET#	RESET	0
	(blank)	1		(blank)	1
RDYRC#	READY	0	NMI#	NMI	0
	(blank)	1		(blank)	1
DEN#	DATA EN	0	HOLD	(blank)	0
	DATA DIS	1		HOLD	1
D/C#	CODE	0	FAIL#	FAIL	0
	DATA	1		(blank)	1
BLAST#	BLAST	0	STEST	(blank)	0
	(blank)	1		STEST	1
LOCK#	LOCK	0	TRST#	TRST	0
	(blank)	1		(blank)	1
DT/R#	RECV	0	WAIT#	WAIT	0
	XMIT	1		(blank)	1

Timing format specification

The i960RP configuration files contain predefined format specifications. Thesame configuration files are used for state and timing.

Chapter 4 of this guide contains a table that lists the signals for the HP E2484A analysis probe and on which analysis probe pod and probe line the signal comes to the logic analyzer. Refer to this table and to the logic analyzer connection information for your analyzer in chapter 2 to determine where the processor signals should be on the timing format specification screen.

To display captured timing data

Timing data is displayed in the Waveform menu of the logic analyzer.
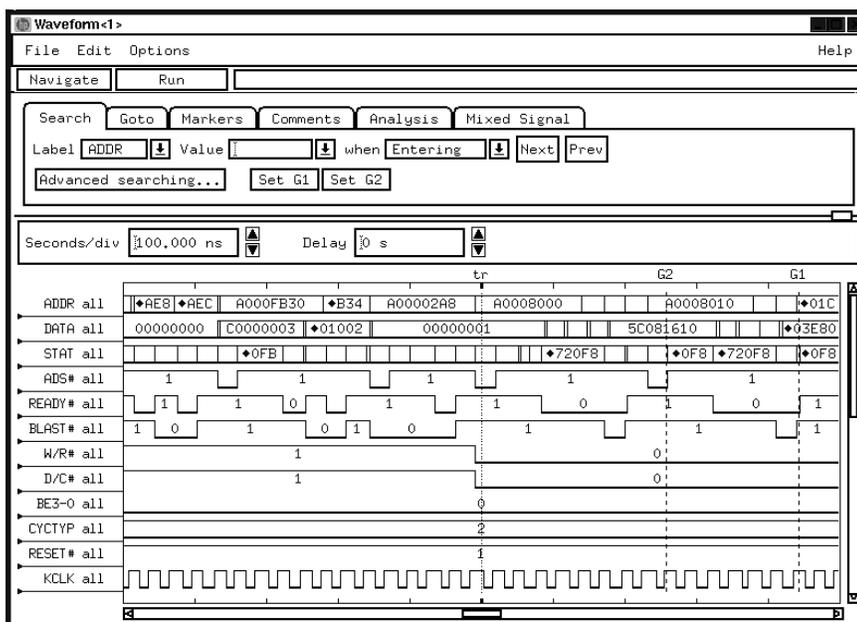
Waveform Menu

Using the Inverse Assemblers

The HP E2484A analysis probe contains four inverse assemblers:
I960R1, I960R2, I960R1E, and I960R2E. The R1 suffix is for little
endian systems, while the R2 suffix is for big endian systems. The
default is to load a little endian inverse assembler.

The E suffix indicates an enhanced version of the inverse assembler.
The enhanced inverse assemblers contain all the functions of the
other inverse assemblers, plus additional features. For information on
the enhanced inverse assembler features, see "The enhanced inverse
assemblers" on page 3-17.

The configuration software checks the logic analyzer during the load
process. If the logic analyzer has the appropriate software version, the
configuration file loads the enhanced inverse assembler. For
information on the logic analyzer operating system version
requirements, refer to "Logic analyzer software version requirements"
on page 1-5.

The following sections describe the features common to all four
inverse assemblers.

To display captured state data

The logic analyzer displays captured data in the Listing menu. The inverse assembler disassembles the captured data in a format that closely resembles the assembly source code for your processor.

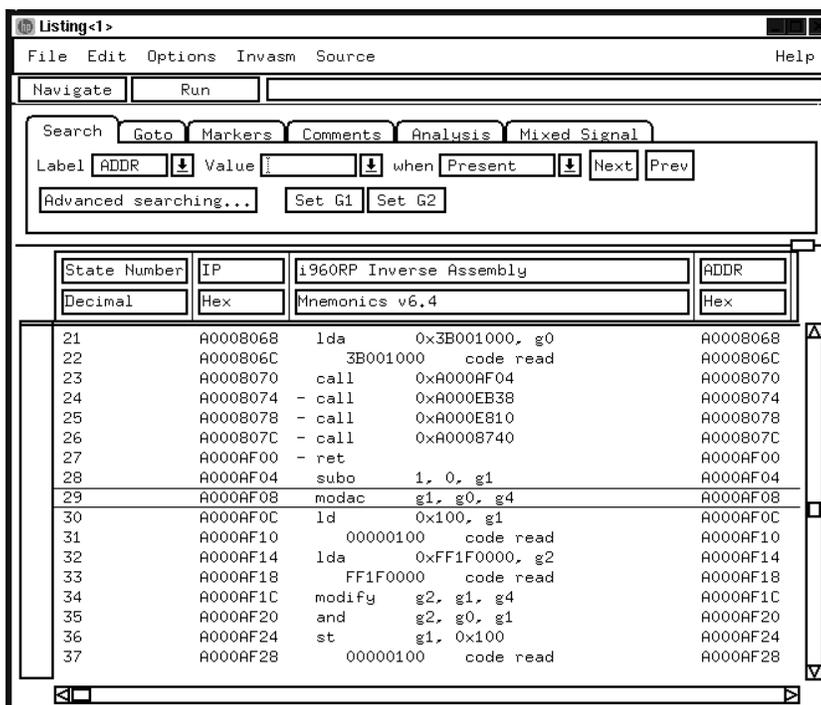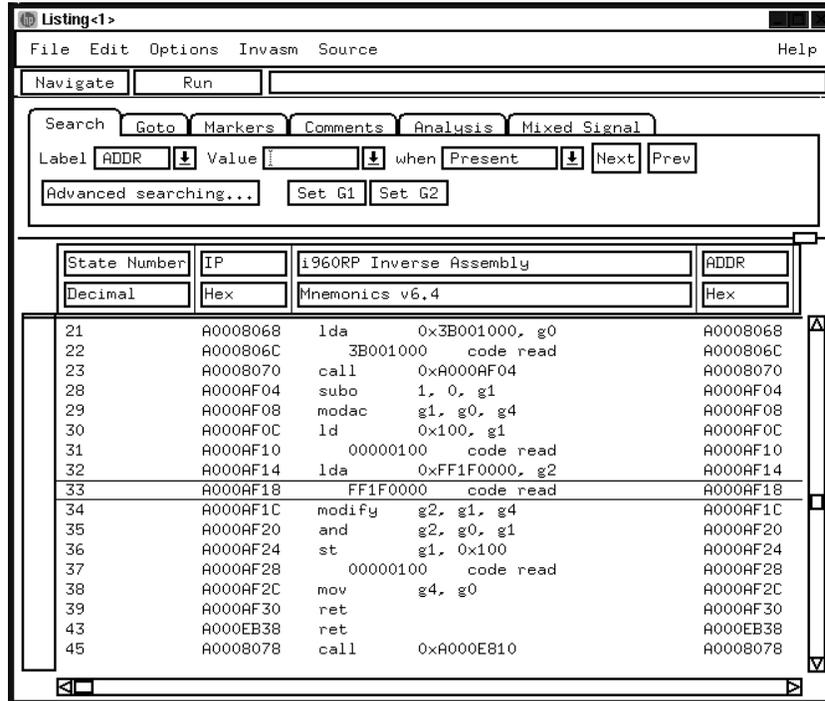If your trace listing doesn't otherwise appear to be correct (capturing the same RAM address twice, for example), make sure the analysis probe hardware is configured for state analysis. The "Invasm" field will appear at the top of the Listing menu screen when the logic analyzer is configured for state analysis. See Chapter 2 to review the hardware configuration, correct it if needed, and then run the trace again.

```
Listing<1>

 File  Edit  Options  Invasm  Source                              Help

  Navigate        Run

  Search    Goto   Markers   Comments   Analysis   Mixed Signal
 Label ADDR    ↓  Value          ↓  when Present      ↓ Next  Prev

  Advanced searching...      Set G1   Set G2

   State Number  IP        i960RP Inverse Assembly            ADDR

   Decimal       Hex       Mnemonics v6.4                     Hex

    21           A0008068   lda      0x3B001000, g0           A0008068
    22           A000806C      3B001000    code read          A000806C
    23           A0008070   call     0xA000AF04               A0008070
    24           A0008074 - call     0xA000EB38               A0008074
    25           A0008078 - call     0xA000E810               A0008078
    26           A000807C - call     0xA0008740               A000807C
    27           A000AF00 - ret                               A000AF00
    28           A000AF04   subo     1, 0, g1                 A000AF04
    29           A000AF08   modac    g1, g0, g4               A000AF08
    30           A000AF0C   ld       0x100, g1                A000AF0C
    31           A000AF10      00000100    code read          A000AF10
    32           A000AF14   lda      0xFF1F0000, g2           A000AF14
    33           A000AF18      FF1F0000    code read          A000AF18
    34           A000AF1C   modify   g2, g1, g4               A000AF1C
    35           A000AF20   and      g2, g0, g1               A000AF20
    36           A000AF24   st       g1, 0x100                A000AF24
    37           A000AF28      00000100    code read          A000AF28
```

Listing Menu, No Suppression

The following figure shows the Listing menu display using the enhanced inverse assembler configured to suppress unused prefetches:

```
┌─────────────────────────────────────────────────────────────────────┐
│ ⦿ Listing<1>                                                  ■■■    │
│                                                                       │
│   File  Edit  Options  Invasm  Source                        Help     │
│  ┌──────────┐ ┌──────────┐ ┌─────────────────────────────────────┐   │
│  │ Navigate │ │   Run    │ │                                     │   │
│  └──────────┘ └──────────┘ └─────────────────────────────────────┘   │
│   ┌Search┐┌─Goto─┐┌─Markers─┐┌─Comments─┐┌─Analysis─┐┌Mixed Signal┐  │
│                                                                       │
│   Label ADDR ↓ Value [        ] ↓ when Present ↓ Next Prev           │
│                                                                       │
│   Advanced searching...    Set G1  Set G2                            │
│                                                                       │
│  ┌──────────────┬───┬──────────────────────────┬──────────┐          │
│  │State Number  │IP │i960RP Inverse Assembly   │ADDR      │          │
│  │Decimal       │Hex│Mnemonics v6.4            │Hex       │          │
│  ├──────────────┴───┴──────────────────────────┴──────────┤         │
│     21       A0008068   lda      0x3B001000, g0    A0008068          │
│     22       A000806C      3B001000    code read    A000806C         │
│     23       A0008070   call     0xA000AF04        A0008070          │
│     28       A000AF04   subo     1, 0, g1          A000AF04          │
│     29       A000AF08   modac    g1, g0, g4        A000AF08          │
│     30       A000AF0C   ld       0x100, g1         A000AF0C          │
│     31       A000AF10      00000100    code read    A000AF10         │
│     32       A000AF14   lda      0xFF1F0000, g2    A000AF14          │
│     33       A000AF18      FF1F0000    code read    A000AF18         │
│     34       A000AF1C   modify   g2, g1, g4        A000AF1C          │
│     35       A000AF20   and      g2, g0, g1        A000AF20          │
│     36       A000AF24   st       g1, 0x100         A000AF24          │
│     37       A000AF28      00000100    code read    A000AF28         │
│     38       A000AF2C   mov      g4, g0            A000AF2C          │
│     39       A000AF30   ret                        A000AF30          │
│     43       A000EB38   ret                        A000EB38          │
│     45       A0008078   call     0xA000E810        A0008078          │
└─────────────────────────────────────────────────────────────────────┘
```

State Listing with Unused Prefetches Suppressed

To use the Invasm key

The inverse assembler may occasionally start disassembly on the extention word of a load immediate instruction. The following steps may be taken to correct this:

- Roll the first word of the load immediate instruction to the top of the listing screen (line 21 in the example above).
- Select the Invasm key.

Inverse assembler output format

The next few paragraphs describe the general output format of the inverse assembler.

Endian Mode

The i960RP normally operates in little endian mode. Some i960 code will switch the microprocessor to big endian mode, and the data captured by the logic analyzer will be in big endian mode. If you want to inverse assemble the big endian data, you must load the big endian inverse assembler (H2 suffix) and apply it to the big endian data.

Numeric Format

Most of the numeric output from the inverse assembler is in hexadecimal format, and is preceded by 0x. Decimal values do not have a prefix.

Missing Opcodes

Asterisks (*) in the inverse assembler output indicate that a portion (or portions) of an instruction was not captured by the analyzer. Missing opcodes occur occasionally, primarily with the load immediate instruction.

Don't Care Bytes

The i960RP microprocessor can perform byte, two-byte, and four-byte transfers between microprocessor registers and memory. Byte transfers can start in any byte on the 32-bit data bus. Two-byte transfers can start on any even-numbered byte (byte 0, 2, 4, . . . E) and four-byte transfers can start on every fourth byte (0, 4, 8, C). The bytes that are valid in a transfer are indicated by the microprocessor BE#s and WIDTH0 and WIDTH1 lines. The inverse assembler displays ".." for any bytes in a transfer that are ignored by the microprocessor. You can determine exactly which byte or bytes of data were used as an operand.

Unexecuted Prefetched Instructions

The analysis probe sends all of the bus transactions by the microprocessor to the logic analyzer. Prefetched instructions which are not executed by the microprocessor are also captured into the state listing.

Inverse assembler error messages

Any of the following list of error messages may appear during analysis of your target software. Included with each message is a brief explanation.

Illegal Task Request   Displayed if the microprocessor is asked to perform a task which it cannot do.

Fatal Data Error   Displayed if the trace memory could not be read properly on entry into the inverse assembler.

Invalid Status   Displayed if the status field for the current state is not valid.

Illegal Opcode   Displayed if the inverse assembler encounters an illegal instruction.

Reserved Opcode   Displayed if the inverse assembler encounters a reserved instruction.

No Operand   Displayed if the inverse assembler cannot find a complete operand field for an instruction. Prefetch activity or storage qualification is often the cause.

The enhanced inverse assemblers

The enhanced inverse assemblers contain all the functions of the other inverse assemblers (see previous sections), plus additional features.

The configuration software checks the logic analyzer during the load process. If the logic analyzer has the appropriate software version, the configuration file loads the enhanced inverse assembler. For information on the logic analyzer operating system version requirements, refer to "Logic analyzer software version requirements" on page 1-5.

The Invasm menu contains four functions: Load (HP 16600/700 only), Filtering with Show/Suppress selections, Align, and Options. The following sections describe these functions.

Load

The Load function lets you load a different inverse assembler and apply it to the data in the Listing menu. You can use Load to change from the big endian inverse assembler to the little endian inverse assembler. In some cases you may have acquired raw data, in which case the Load function lets you apply an inverse assembler to that data.

Filter

The Filter function brings up a Show/Suppress menu. You can change the settings to specify whether the various microprocessor operations are shown or suppressed on the logic analyzer display. The following figure shows the microprocessor operations which have this option. The settings for the various operations do not affect the data which is stored by the logic analyzer, they only affect whether that data is displayed or not. The same data can be examined with different settings, for different analysis requirements.

This function allows faster analysis in two ways. First, unneeded information can be filtered out of the display. Suppressing unexecuted prefetches, for an example, will show only instructions that are executed by the i960 CPU.

Second, particular operations can be isolated by suppressing all other operations. For example, data Read/Write can be shown, with all other operations suppressed, allowing quick analysis of Read/Write operations.

The following figure shows the Filter menu.

```
┌─────────────────────────────────────────┐
│ ⓗ Invasm Filter – Listing<1>        [✕] │
│        80960RP Filter Options            │
│        Frame 10:Slot E:i960RP            │
│ ─────────────────────────────────────── │
│ Code Reads                               │
│   Unexecuted Prefetches: ┌──────────┐    │
│                          │ Show    ▣│    │
│                          └──────────┘    │
│   Probable Prefetches:   ┌──────────┐    │
│                          │ Show    ▣│    │
│                          └──────────┘    │
│   Jumps:                 ┌──────────┐    │
│                          │ Show    ▣│    │
│                          └──────────┘    │
│   Calls and Returns:     ┌──────────┐    │
│                          │ Show    ▣│    │
│                          └──────────┘    │
│   Other Instructions:    ┌──────────┐    │
│                          │ Show    ▣│    │
│                          └──────────┘    │
│ Memory Reads:            ┌──────────┐    │
│                          │ Show    ▣│    │
│                          └──────────┘    │
│ Memory Writes:           ┌──────────┐    │
│                          │ Show    ▣│    │
│                          └──────────┘    │
│ ─────────────────────────────────────── │
│   ┌───────┐   ┌───────┐    ┌───────┐     │
│   │ Apply │   │ Reset │    │ Close │     │
│   └───────┘   └───────┘    └───────┘     │
└─────────────────────────────────────────┘
```
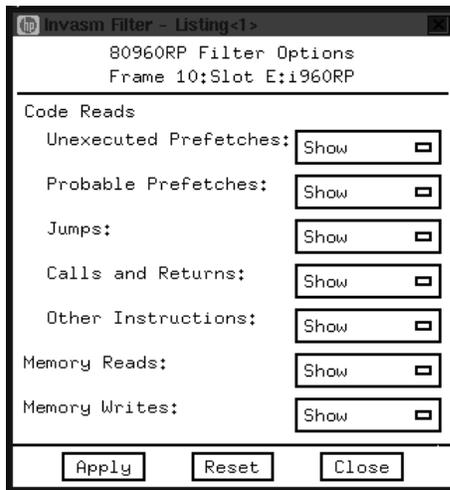
Filter Menu

If the X or O pattern markers are turned on, and the designated pattern is found in a state that has been Suppressed with display filtering, the following message will appear on the logic analyzer display: "X (or O) pattern found, but state is suppressed."

Align

Align enables the inverse assembler to re-align with the microprocessor code. In some cases the prefetch marking algorithm in the inverse assembler may lose synchronization, and unused prefetches or executed instructions may be incorrectly marked. If any of the Code Reads are suppressed, this could cause some executed instructions to be missing from the display.

To align the inverse assembler, roll the first incorrectly marked state to the top of the listing screen, then click Align.

Options

The Options menu lets you change the width of the display.

Reference

Reference

This chapter contains additional reference information including the signal mapping for the HP E2484A analysis probe.

The information in this chapter is presented in the following sections:

- Operating characteristics
- Theory of operation and clocking
- Signal-to-connector mapping
- Circuit board dimensions
- Replaceable parts
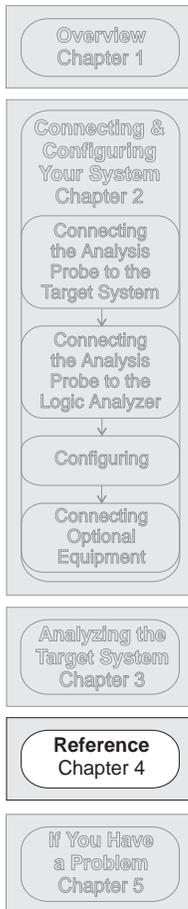
Operating characteristics

The following operating characteristics are not specifications, but are typical operating characteristics for the analysis probe.

Operating Characteristics

Microprocessor Compatibility	Intel 80960RP microprocessor. Both 5 V and 3.3 V versions are supported.
Microprocessor Package	352-pin BGA, with built-in Intel P2P connector
Microprocessor Clock Speed	33 MHz maximum
Accessories Required	None
Power Requirements	1.0 A at +5 Vdc maximum, supplied by the logic analyzer. CAT I, Pollution degree 2.
Logic Analyzer Required	HP 1660A/AS/C/CS/CP, HP 1661A/AS/C/CS/CP, HP 1670A/D, HP 1671A/D, HP 16550A (one card), HP 16554A/55A/56A (two cards), HP 16555D/56D (two cards), HP 16600A, HP 16601A, HP 16602A
Probes Required	Five 16-channel pods are required for inverse assembly. A sixth pod contains additional signals you might want to monitor.
Signal Line Loading	Approximately 24 pF on ADS# and RDYRCV#. Approximately 16 pF on all other signals.
Timing Analysis	All signals are buffered by a 74FCT646ATQ gate with a 1-ns channel-to-channel skew except for TMS, TDI, TDO, and TCLK, which are not bufferred. ADDR signals are the duplicates of DATA signals, except that ADDR signals are bufferred by two 74FCT646ATQ gates.
Environmental Temperature	Operating 0 to 55 degrees C (+32 to +131 degrees F) Nonoperating -40 to +75 degrees C (-40 to +167 degrees F)
Altitude	Operating 4,600 m (15,000 ft) Nonoperating 15,300 m (50,000 ft)
Humidity	Up to 90% noncondensing. Avoid sudden, extreme temperature changes which could cause condensation within the instrument.

Theory of operation and clocking

The figure on the following page shows a block diagram of the HP E2484A analysis probe.

The E2484A analysis probe has three modes of operations: State-per-transfer, State-per-clock, and Timing. Timing mode is selected with the State/Timing switch, and State-per-transfer and State-per-clock are selected by the choice of clocking.

There are two switches on the E2484A analysis probe. Switch 1 selects the frequency range. Set it to HIGH if the CPU clkin frequency is 10 MHz or higher and set it to LOW if the frequency is below 10 MHz.

Switch 2 changes the analysis probe between the state and timing mode. Setting switch 2 to OFF places the analysis probe in the state mode. In this mode, the address/data bus is demultiplexed and the address, data, and status information are aligned and fed to the logic analyzer on pods 1, 2, 3, and 4 respectively.

Setting switch 2 to ON causes all of the buffers to behave as flow-through devices. The address signals in this case are simply the duplicate of the data signals with an additional 4 ns delay.

Address 0 and 1

Address 0 and 1 are generated by the pal on the analysis probe from BE0#, BE1#, WIDTH/HLTD0, and WIDTH/HLTD1.

Addr0 = (!WIDTH/HLTD1 & !WIDTH/HLTD0) & BE0#
Addr1 = [(!WIDTH/HLTD1 & !WIDTH/HLTD0)#(!WIDTH/HLTD1 &
　　　　　WIDTH/HLTD0)] & BE1#
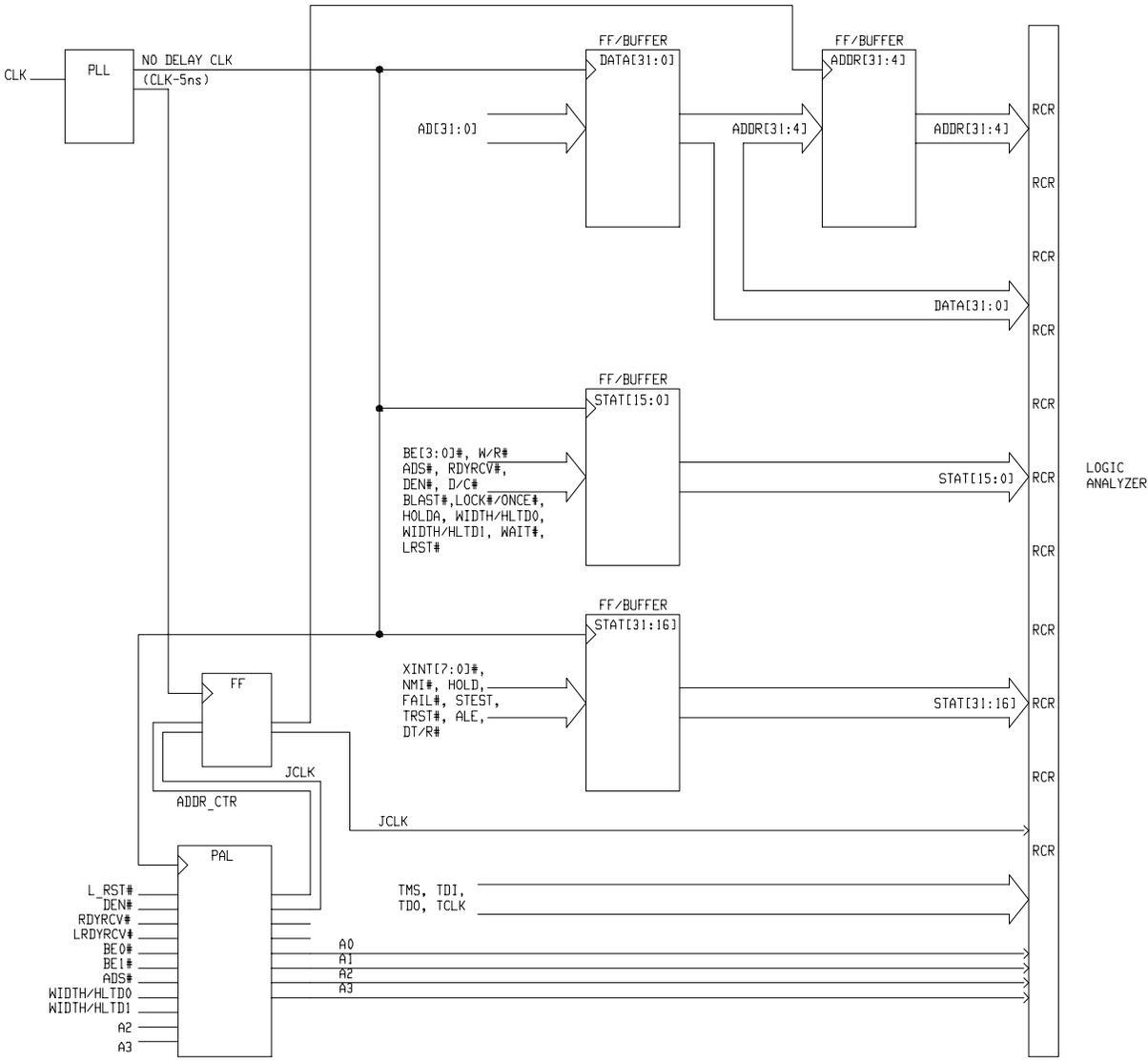
Block Diagram

Timing Mode

In timing mode, all signals are flow-through and have approximately 1 ns channel-to-channel skew. The address signals lag the data signals by about 4 ns since the address signals have to go through two buffers instead of one. The figure below shows the waveform diagram.

In the timing mode, all signals have a 4 ns delay with respect to the CPU signals except for TMS, TDO, TDI, and TCLK which have 0 ns delay.

i960RP TIMING WAVEFORM
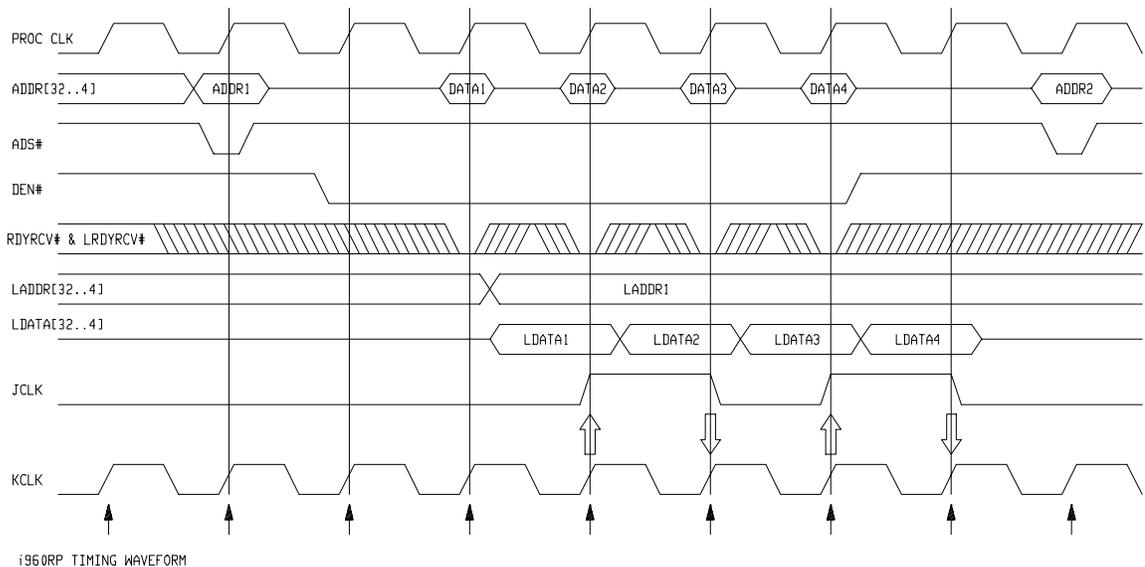
Waveform Diagram

Signal-to-connector mapping

The following table shows the signal-to-connector mapping. The signal list
table column descriptions are as follows:

POD	The analysis probe pod the signal that carries the signal.
LA PROBE	The probe within the pod that carries the signal.
PIN NAME	The microprocessor pin name.
E2484A PIN	The analysis probe PGA socket pin number for the signal.
BGA PIN	The microprocessor pin number for the signal.
LABEL	The analyzer label assigned to the signal.
ALT LABEL	An additional label also assigned to the signal (if any).

i960RP Signal List

POD	LA PROBE	PIN NAME	E2484A PIN	BGA PIN	LABEL	ALT LABEL
P1	0	A0			ADDR	
P1	1	A1			ADDR	
P1	2	A2	C5	C17	ADDR	
P1	3	A3	C4	A17	ADDR	
P1	4	AD4	M13	B17	ADDR	
P1	5	AD5	L12	C16	ADDR	
P1	6	AD6	P14	A16	ADDR	
P1	7	AD7	N13	B16	ADDR	
P1	8	AD8	M12	C15	ADDR	
P1	9	AD9	M11	A15	ADDR	
P1	10	AD10	N12	B15	ADDR	
P1	11	AD11	P13	C14	ADDR	
P1	12	AD12	M10	A14	ADDR	
P1	13	AD13	P12	B14	ADDR	
P1	14	AD14	M9	C13	ADDR	
P1	15	AD15	M8	A13	ADDR	
P1	CLK (generated by the analysis probe)				JCLK	

i960RP Signal List (continued)

POD	LA PROBE	PIN NAME	E2484A PIN	BGA PIN	LABEL	ALT LABEL
P2	0	AD16	M7	B13	ADDR	
P2	1	AD17	M6	C12	ADDR	
P2	2	AD18	P4	A12	ADDR	
P2	3	AD19	P3	B12	ADDR	
P2	4	AD20	N4	C11	ADDR	
P2	5	AD21	M5	A11	ADDR	
P2	6	AD22	P2	B11	ADDR	
P2	7	AD23	M4	C10	ADDR	
P2	8	AD24	N3	A10	ADDR	
P2	9	AD25	P1	B10	ADDR	
P2	10	AD26	N2	C9	ADDR	
P2	11	AD27	N1	A9	ADDR	
P2	12	AD28	L2	B9	ADDR	
P2	13	AD29	M2	C8	ADDR	
P2	14	AD30	M1	A8	ADDR	
P2	15	AD31	K3	B8	ADDR	
P2	CLK	CLKIN	H14	F25	KCLK	

i960RP Signal List (continued)

POD	LA PROBE	PIN NAME	E2484A PIN	BGA PIN	LABEL	ALT LABEL
P3	0	AD0	M14	A18	DATA	
P3	1	AD1	L13	B18	DATA	
P3	2	AD2	K12	C17	DATA	
P3	3	AD3	N14	A17	DATA	
P3	4	AD4	M13	B17	DATA	
P3	5	AD5	L12	C16	DATA	
P3	6	AD6	P14	A16	DATA	
P3	7	AD7	N13	B16	DATA	
P3	8	AD8	M12	C15	DATA	
P3	9	AD9	M11	A15	DATA	
P3	10	AD10	N12	B15	DATA	
P3	11	AD11	P13	C14	DATA	
P3	12	AD12	M10	A14	DATA	
P3	13	AD13	P12	B14	DATA	
P3	14	AD14	M9	C13	DATA	
P3	15	AD15	M8	A13	DATA	
P3	CLK	TCK	B13	B24	TCK	

i960RP Signal List (continued)

POD	LA PROBE	PIN NAME	E2484A PIN	BGA PIN	LABEL	ALT LABEL
P4	0	AD16	M7	B13	DATA	
P4	1	AD17	M6	C12	DATA	
P4	2	AD18	P4	A12	DATA	
P4	3	AD19	P3	B12	DATA	
P4	4	AD20	N4	C11	DATA	
P4	5	AD21	M5	A11	DATA	
P4	6	AD22	P2	B11	DATA	
P4	7	AD23	M4	C10	DATA	
P4	8	AD24	N3	A10	DATA	
P4	9	AD25	P1	B10	DATA	
P4	10	AD26	N2	C9	DATA	
P4	11	AD27	N1	A9	DATA	
P4	12	AD28	L3	B9	DATA	
P4	13	AD29	M2	C8	DATA	
P4	14	AD30	M1	A8	DATA	
P4	15	AD31	K3	B8	DATA	
P4	CLK	TDI	D12	D26	TDI	

i960RP Signal List (continued)

POD	LA PROBE	PIN NAME	E2484A PIN	BGA PIN	LABEL	ALT LABEL
P5	0	BE0#	H3	A22	STAT	BE#
P5	1	BE1#	J3	B22	STAT	BE#
P5	2	BE2#	L1	C21	STAT	BE#
P5	3	BE3#	L2	A21	STAT	BE#
P5	4	W/R#	B1	C22	STAT	W/R#
P5	5	ADS#	A1	B21	STAT	ADS#
P5	6	RDYRCV#	F12	B19	STAT	RDYRCV#
P5	7	DEN#	E3	A23	STAT	DEN#
P5	8	D/C#	B2	AF4	STAT	D/C#
P5	9	BLAST#	C3	C23	STAT	BLAST#
P5	10	LOCK#/ONCE#	C1	AD4	STAT	LOCK#/ONCE#
P5	11	HOLDA	C2	V3	STAT	HOLDA
P5	12	WIDTH/HLTD0	B3	AF5	STAT	WIDTH
P5	13	WIDTH/HLTD1	A2	AE5	STAT	WIDTH
P5	14	WAIT#	A3	N3	STAT	WAIT#
P5	15	RESET#	E12	AD6	STAT	RESET#
P5	CLK	TDO	B4	D25	TDO	

i960RP Signal List (continued)

POD	LA PROBE	PIN NAME	E2484A PIN	BGA PIN	LABEL	ALT LABEL
P6	0	XINT0#	C11	N1	XINT	
P6	1	XINT1#	C10	N2	XINT	
P6	2	XINT2#	A13	P3	XINT	
P6	3	XINT3#	B12	P1	XINT	
P6	4	XINT4#	B11	P2	XINT	
P6	5	XINT5#	A12	R3	XINT	
P6	6	XINT6#	B10	R1	XINT	
P6	7	XINT7#	A11	R2	XINT	
P6	8	NMI#	A10	T3	NMI#	
P6	9	HOLD	C9	V1	HOLD	
P6	10	FAIL#	C6	AD5	FAIL#	
P6	11	STEST	C13	AE3	STEST	
P6	12	TRST#	C12	C25	TRST#	
P6	13	ALE	G3	C20	ALE	
P6	14	nc	F3	nc		
P6	15	DT/R#	D3	B23	DT/R#	
P6	CLK	TMS	A14	C24	TMS	

Circuit board dimensions

The following illustration gives the dimensions for the analysis probe assembly. The dimensions are listed in inches and millimeters.

3.200 in
81.28 mm

3.116 in
79.15 mm

0.286 in
7.264 mm
(does not include target board thickness)

1.734 in
44.04 mm

e2484e02
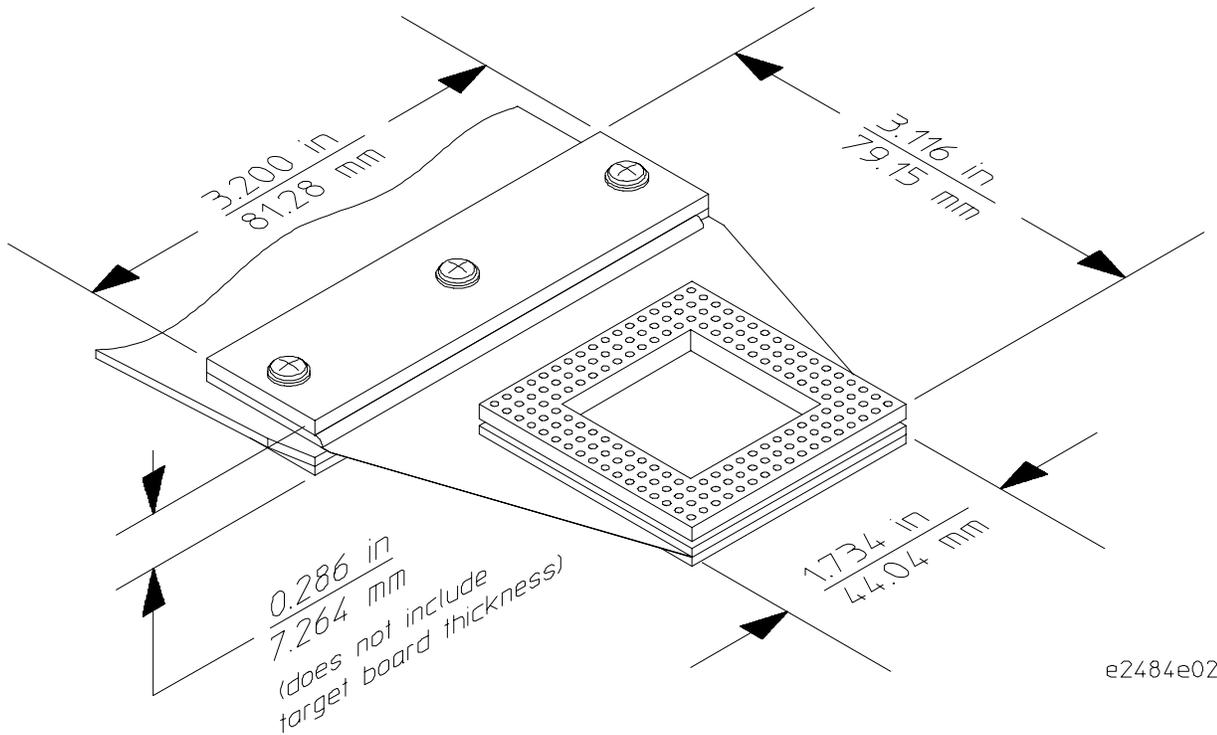
Dimensions

Replaceable parts

The repair strategy for this analysis probe is board replacement. However, the following table lists some mechanical parts that may be replaced if they are damaged or lost. Contact your nearest Hewlett-Packard Sales Office for further information on servicing the board.

Exchange assemblies are available when a repairable assembly is returned to Hewlett-Packard. These assemblies have been set up on the "Exchange Assembly" program. This allows you to exchange a faulty assembly with one that has been repaired, calibrated, and performance verified by the factory. The cost is significantly less than that of a new assembly.

Replaceable Parts

HP Part Number	Description
E2484-69501	Circuit board assembly
E2484-68700	Inverse assembler disk pouch
1200-1605	PGA pin protector socket
E2484-66502	P2P Adapter Assembly

If You Have a Problem

If You Have a Problem
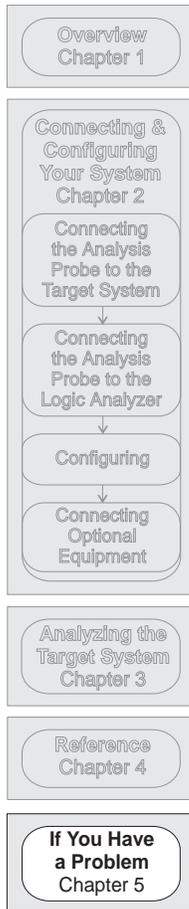
Occasionally, a measurement may not give the expected results. If you encounter difficulties while making measurements, use this chapter to guide you through some possible solutions. Each heading lists a problem you may encounter, along with some possible solutions.

The information in this chapter is presented in the following sections:

- Logic analyzer problems
- Analysis probe problems
- Inverse assembler problems
- Intermodule measurement problems
- Messages
- Cleaning the instrument

If you still have difficulty after trying the suggestions in this chapter, contact your local Hewlett-Packard Service Center.

CAUTION   When you are working with the analyzer, be sure to power down both the analyzer and the target system before disconnecting or connecting cables, probes, and analysis probes. Otherwise, you may damage circuitry in the analyzer, analysis probe, or target system.

Analyzer Problems

This section lists general problems that you might encounter while using the analyzer.

Intermittent data errors

This problem is usually caused by poor connections, incorrect signal levels, or marginal timing.

☐ Remove and reseat all cables and probes, ensuring that there are no bent pins on the analysis probe or poor probe connections.

☐ Adjust the threshold level of the data pod to match the logic levels in the system under test.

☐ Use an oscilloscope to check the signal integrity of the data lines.

Clock signals for the state analyzer must meet particular pulse shape and timing requirements. Data inputs for the analyzer must meet pulse shape and setup and hold time requirements.

See Also See "Capacitive loading" in this chapter for information on other sources of intermittent data errors.

Unwanted triggers

Unwanted triggers can be caused by instructions that were fetched but not executed.

☐ Add the prefetch queue or pipeline depth to the trigger address to avoid this problem.

The logic analyzer captures prefetches, even if they are not executed. When you are specifying a trigger condition or a storage qualification that follows an instruction that may cause branching, an unused prefetch may generate an unwanted trigger.

No activity on activity indicators

☐ Check for loose cables, board connections, and analysis probe connections.

☐ Check for bent or damaged pins on the analysis probe.

No trace list display

If there is no trace list display, it may be that your trigger specification is not correct for the data you want to capture, or that the trace memory is only partially filled.

☐ Check your trigger sequencer specification to ensure that it will capture the events of interest.

☐ Try stopping the analyzer; if the trace list is partially filled, this should display the contents of trace memory.

Analyzer won't power up

If the logic analyzer power is powered down when it is connected to a powered-up target system, the logic analyzer may not be able to power up. Some logic analyzers are inhibited from powering up when they are connected to a target system that is already powered up.

☐ Disconnect all logic analyzer cabling from the analysis probe. This will allow the logic analyzer to power up. Reconnect logic analyzer cabling after power up.

Analysis Probe Problems

This section lists problems that you might encounter when using an analysis probe. If the solutions suggested here do not correct the problem, you may have a damaged analysis probe. Contact your local Hewlett-Packard Sales Office if you need further assistance.

Target system will not boot up

If the target system will not boot up after connecting the analysis probe, the microprocessor (if socketed) or the analysis probe may not be installed properly, or they may not be making electrical contact.

☐ Ensure that you are following the correct power-on sequence for the analysis probe and target system.

1 Power up the analyzer and analysis probe.

2 Power up the target system.

If you power up the target system before you power up the analysis probe, interface circuitry in the analysis probe may latch up and prevent proper target system operation.

☐ Verify that the microprocessor and the analysis probe are properly rotated and aligned so that the index pin on the microprocessor (pin 1 or pin A1) matches the index pin on the analysis probe.

☐ Verify that the microprocessor and the analysis probe are securely inserted into their respective sockets.

☐ Verify that the logic analyzer cables are in the proper sockets of the analysis probe and are firmly inserted.

Erratic trace measurements

There are several general problems that can cause erratic variations in trace lists and inverse assembly failures.

☐ **Do a full reset of the target system before beginning the measurement.**

Some analysis probe designs require a full reset to ensure correct configuration.

☐ **Ensure that your target system meets the timing requirements of the processor with the analysis probe installed.**

See "Capacitive Loading" in this chapter. While analysis probe loading is slight, pin protectors, extenders, and adapters may increase it to unacceptable levels. If the target system design has close timing margins, such loading may cause incorrect processor functioning and give erratic trace results.

☐ **Ensure that you have sufficient cooling for the microprocessor.**

Some microprocessors generate substantial heat. This is exacerbated by the active circuitry on the analysis probe board. You should ensure that you have ambient temperature conditions and airflow that meet or exceed the requirements of the microprocessor manufacturer.

Capacitive loading

Excessive capacitive loading can degrade signals, resulting in incorrect capture by the analysis probe, or system lockup in the microprocessor. All analysis probes add additional capacitive loading, as can custom probe fixtures you design for your application.

Careful layout of your target system can minimize loading problems and result in better margins for your design. This is especially important for systems that are running at frequencies greater than 50 MHz.

☐ **Remove as many pin protectors, extenders, and adapters as possible.**

☐ **If multiple analysis probe solutions are available, use one with lower capacitive loading.**

Inverse Assembler Problems

This section lists problems that you might encounter while using the inverse assembler.

When you obtain incorrect inverse assembly results, it may be unclear whether the problem is in the analysis probe or in your target system. If you follow the suggestions in this section to ensure that you are using the analysis probe and inverse assembler correctly, you can proceed with confidence in debugging your target system.

No inverse assembly or incorrect inverse assembly

This problem may be due to incorrect alignment, modified configuration files, incorrect connections, or a hardware problem in the target system. A locked status line can cause incorrect or incomplete inverse assembly.

☐ Ensure that each logic analyzer pod is connected to the correct analysis probe connector.

There is not always a one-to-one correspondence between analyzer pod numbers and analysis probe cable numbers. Microprocessor interfaces must supply address (ADDR), data (DATA), and status (STAT) information to the analyzer in a predefined order. The cable connections for each analysis probe are often altered to support that need. Thus, one analysis probe might require that you connect cable 2 to analyzer pod 2, while another will require you to connect cable 5 to analyzer pod 2. See Chapter 2 for connection information.

☐ Check the activity indicators for status lines locked in a high or low state.

☐ Verify that the STAT, DATA, and ADDR format labels have not been modified from their default values.

These labels must remain as they are configured by the configuration file. Do not change the names of these labels or the bit assignments within the labels. Some analysis probes also require other data labels. See Chapter 3 for more information.

☐ Verify that all microprocessor caches and memory managers have been disabled.

In most cases, if the microprocessor caches and memory managers remain enabled you should still get inverse assembly. It may be incorrect because a portion of the execution trace was not visible to the logic analyzer.

☐ Verify that storage qualification has not excluded storage of all the needed opcodes and operands.

Inverse assembler will not load or run

You need to ensure that you have the correct system software loaded on your analyzer.

☐ For the HP 16600/700 logic analysis systems, the inverse assembler must be installed on the hard drive using the procedures listed on the jacket for the CD-ROM. Re-install the Processor Support Package for this product, then try loading the configuration file again.

☐ For other logic analyzers, ensure that the inverse assembler is on the same disk as the configuration files you are loading.

Configuration files for the state analyzer contain a pointer to the name of the corresponding inverse assembler. If you delete the inverse assembler, rename it, or use the File Manager Copy command to copy it to the HP 16600/700 logic analysis systems, the configuration process will fail to load the inverse assembler.

See Chapter 3 for details.

Intermodule Measurement Problems

Some problems occur only when you are trying to make a measurement involving multiple modules.

An event wasn't captured by one of the modules

If you are trying to capture an event that occurs very shortly after the event that arms one of the measurement modules, it may be missed due to internal analyzer delays. For example, suppose you set the oscilloscope to trigger upon receiving a trigger signal from the logic analyzer because you are trying to capture a pulse that occurs right after the analyzer's trigger state. If the pulse occurs too soon after the analyzer's trigger state, the oscilloscope will miss the pulse.

☐ Adjust the skew in the Intermodule menu.

You may be able to specify a skew value that enables the event to be captured.

☐ Change the trigger specification for modules upstream of the one with the problem.

If you are using a logic analyzer to trigger the scope, try specifying a trigger condition one state before the one you are using. This may be more difficult than working with the skew because the prior state may occur more often and may not always be related to the event you are trying to capture with the oscilloscope.

Analyzer Messages

This section lists some of the messages that the analyzer displays when it encounters a problem.

". . . Enhanced Inverse Assembler Not Found"

This error only occurs on the HP 16600/700 logic analysis systems. This error occurs if you rename or delete the enhanced inverse assembler file that is attached to the configuration file, or if you do not properly install the inverse assembler file on the hard disk. Ensure that the inverse assembler file is not renamed or deleted. If you use the File Manager Copy command to copy an inverse assembler to the HP 16600/700 logic analysis systems, the enhanced inverse assembler will not load. Use the Install procedures listed on the jacket of the CD-ROM to install the files for this product.

". . . Inverse Assembler Not Found"

This error occurs if you rename or delete the inverse assembler file that is attached to the configuration file. Ensure that the inverse assembler file is not renamed or deleted.

For the HP 16600/700 logic analysis systems, the inverse assembler must be installed on the hard drive using the procedures listed on the jacket for the CD-ROM.

For other logic analyzers, if you have copied the files to the logic analyzer hard disk, ensure that the inverse assembler is located in the same directory as the configuration file.

". . . Does Not Appear to be an Inverse Assembler File"

This error occurs if the inverse assembler file requested by the configuration file is not a valid inverse assembler. Use the Install procedures listed on the jacket of the CD-ROM to re-install the files for this product.

"Measurement Initialization Error"

This error occurs when you have installed the cables incorrectly on logic analysis cards. The following diagrams show the correct cable connections for one-card and two-card HP 16550A installations. Ensure that your cable connections match the silk screening on the card, and that they are fully seated in the connectors. Then, repeat the measurement.
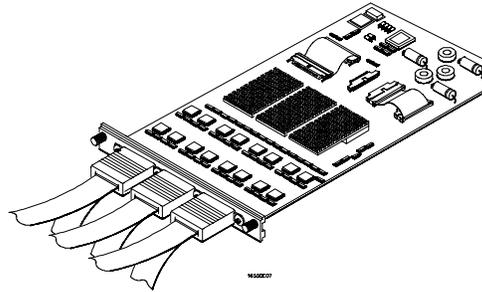
Cable Connections for One-Card HP 16550A Installations
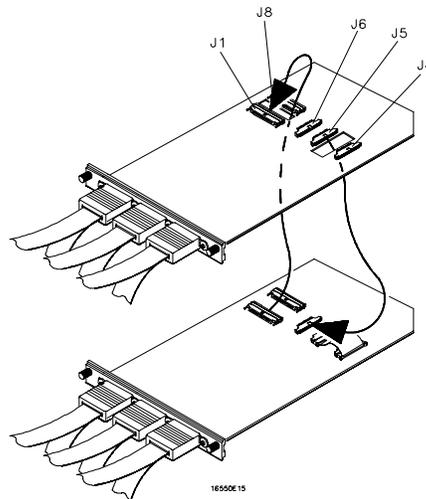
Cable Connections for Two-Card HP 16550A Installations

See Also   The *HP 16550A 100-MHz State/500-MHz Timing Logic Analyzer Service Guide*.

The following diagrams show the correct cable connections for one-card, two-card, and three-card installations on HP 16554A, HP 16555A/D, and HP 16556A/D logic analysis cards. Ensure that your cable connections match the silk screening on the card, and that they are fully seated in the connectors. Then, repeat the measurement.
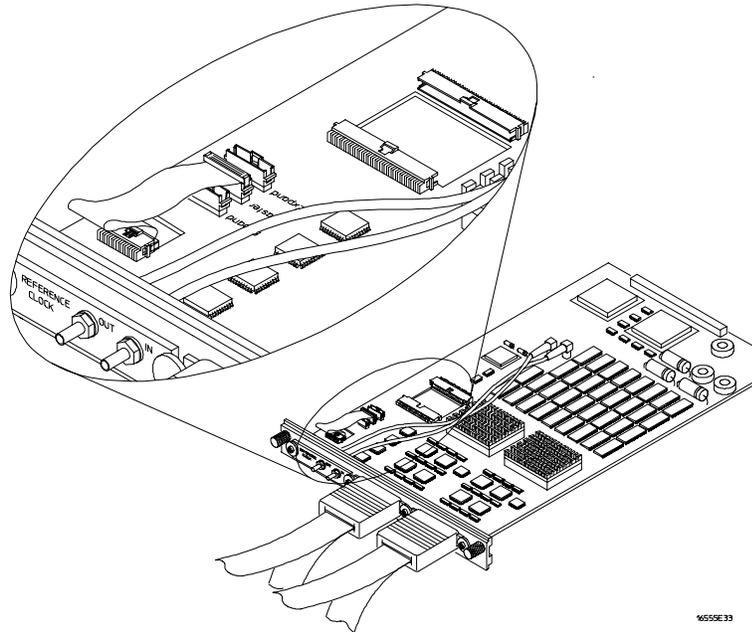
Cable Connections for One-Card HP 16554/55/56 Installations

16554E06
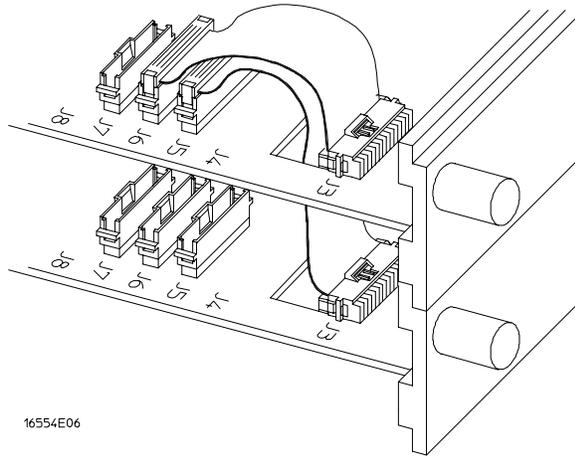
Cable Connections for Two-Card HP 16554/55/56 Installations

16555E36
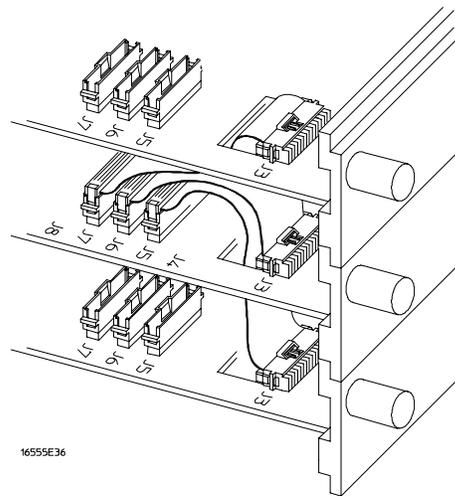
Cable Connections for Three-Card HP 16554/55/56 Installations

See Also   *The HP 16554A 70-MHz State/250-MHz Timing Logic Analyzer Service Guide.*

The HP 16555A 110-MHz State/250-MHz Timing Logic Analyzer Service Guide.

The HP 16556A 100-MHz State/400-MHz Timing Logic Analyzer Service Guide.

"No Configuration File Loaded"

This is usually caused by trying to load a configuration file for one type of module/system into a different type of module/system.

☐ Verify that the appropriate module has been selected from the Load {module} from File {filename} in the HP 16500A/B/C disk operation menu. Selecting Load {All} will cause incorrect operation when loading most analysis probe configuration files.

See Also   Chapter 2 describes how to load configuration files.

"Selected File is Incompatible"

This occurs when you try to load a configuration file for the wrong module. Ensure that you are loading the appropriate configuration file for your logic analyzer.

"Slow or Missing Clock"

☐ This error message might occur if the logic analyzer cards are not firmly seated in the logic analysis system mainframe. Ensure that the cards are firmly seated.

☐ This error might occur if the target system is not running properly. Ensure that the target system is on and operating properly.

☐ If the error message persists, check that the logic analyzer pods are connected to the proper connectors on the analysis probe. See Chapter 2 to determine the proper connections.

"Time from Arm Greater Than 41.93 ms"

The state/timing analyzers have a counter to keep track of the time from when an analyzer is armed to when it triggers. The width and clock rate of this counter allow it to count for up to 41.93 ms before it overflows. Once the counter has overflowed, the system does not have the data it needs to calculate the time between module triggers. The system must know this time to be able to display data from multiple modules on a single screen.

"Waiting for Trigger"

If a trigger pattern is specified, this message indicates that the specified trigger pattern has not occurred. Verify that the triggering pattern is correctly set.

☐ When analyzing microprocessors that fetch only from word-aligned addresses, if the trigger condition is set to look for an opcode fetch at an address not corresponding to a word boundary, the trigger will never be found.

Cleaning the Instrument

If this instrument requires cleaning, disconnect it from all power sources and clean it with a mild detergent and water. Make sure the instrument is completely dry before reconnecting it to a power source.

Glossary

Analysis Probe   A probe connected to the target microprocessor. It provides an interface between the signals of the target microprocessor and the inputs of the logic analyzer.

Connector Board   A board whose only function is to provide connections from one location to another. One or more connector boards might be stacked to raise a probe above a target micoprocessor to avoid mechanical contact with other components installed close to the target microprocessor.

Elastomeric Probe Adapter   A connector that is fastened on top of a target microprocessor using a retainer and knurled nut. The conductive elastomer on the bottom of the probe adapter makes contact with pins of the target microprocessor and delivers their signals to connection points on top of the probe adapter.

Emulation Module   An emulation module is installed within the mainframe of a logic analyzer. It provides run control within an emulation and analysis test setup. See Emulation Probe.

Emulation Probe   An emulation probe is a stand-alone instrument connected to the mainframe of a logic analyzer. It provides run control within an emulation and analysis test setup. See Emulation Module.

Flexible Adapter   Two connection devices coupled with a flexible cable. Used for connecting probing hardware on the target microprocessor to the analysis probe.

General-purpose Flexible Adapter A cable assembly that connects the signals from an elastomeric probe adapter to an analysis probe. Normally, a male-to-male header or transition board makes the connections from the general-purpose flexible adapter to the analysis probe.

High-Density Adapter Cable   A cable assembly that delivers signals from an analysis probe hardware interface to the logic analyzer pod cables. A high-density adapter cable has a single Mictor connector that is installed into the analysis probe, and two cables that are connected to corresponding odd and even logic analyzer pod cables.

High Density Termination Adapter Cable   Same as a High Density Adapter Cable, except it has a termination in the Mictor connector.

Jumper   Moveable direct electrical connection between two points.

Mainframe Logic Analyzer   A logic analyzer that resides on one or more board assemblies installed in an HP 16500B/C, 1660xA, or 16700A mainframe.

Male-to-male Header   A board assembly that makes point-to-point connections between the female pins of a flexible adapter or transition board and the female pins of an analysis probe.

Preprocessor Interface   See Analysis Probe.

Preprocessor Probe   See Analysis Probe.

Probe adapter   See Elastomeric Probe Adapter.

Processor Probe   See Emulation Probe and Emulation Module.

Prototype Analyzer   The HP 16505A prototype analyzer acts as an analysis and display processor for the HP 16500B/C logic analysis system. It provides a windowed interface and powerful analysis capabilities.

Setup Assistant   A software program that guides you through the process of connecting and configuring an analysis probe and logic analyzer to make measurements on a specific microprocessor.

Shunt Connector.   See Jumper.

Stand-alone Logic Analyzer   A stand-alone logic analyzer has a pre-defined set of hardware components which provide a specific set of capabilities. It is designed to perform logic analysis. A stand-alone logic analyzer differs from a mainframe logic analyzer in that it does not offer card slots for installation of additional capabilities, and its specifications are not modified based upon selection from a set of optional hardware boards that might be installed within its frame.

Transition Board   A board assembly that obtains signals connected to one side and re-arranges them in a different order for delivery at the other side of the board.

1/4-Flexible Adapter   An adapter that obtains one-quarter of the signals from an elastomeric probe adapter (one side of a target microprocessor) and makes them available for probing.

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Safety Symbols

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